S E C T I O N T H R E E

```
                    40100          ORG   16448
40100   0500 00 0 45123  SECT3     CLA   INTL1+1
40101   0601 00 0 00001            STO   1
40102   0774 00 4 40103            AXT   *+1,4
40103   0636 00 4 00101            SCA   SVXR4,4
40104   0020 00 0 40106            TRA   SI1

        CHECKING POD 04 SI INST FOR FALSE TRAPPING

40105   635147234260               BCD   1TRPCK
40106   0074 00 4 45152  SI1       TSX   CLEAR,4
40107   0774 00 2 40126            AXT   TRPRT,2    ADJUSTING TRAPS FOR
40110   0634 00 2 45202            SXA   TRAPS,2    RETURN IN CASE OF TRAP.
40111   0774 00 1 00013            AXT   11,1       LOAD XRA FOR XEC.
40112  -0754 00 0 00000            PXD               CLEAR ACC
40113   0500 00 0 45122            CLA   INTL1       INITIALIZING LOC
40114   0601 00 0 00000            STO               00000 EACH LOOP.
40115   0760 00 0 00007            ETM               TRAP ON ERROR...

40116   0522 00 1 40176  SI1A      XEC   SIIT+11,1  XEC 11 SI INST.

40117  -0760 00 0 00007            LTM               ENTRY IF ROUT DIDNT TRAP.

                                CHKING LOC 00000 FOR IND OF AN ERROR.
40120   0500 00 0 00000            CLA               LOCATION 00000.
40121   0402 00 0 45122            SUB   INTL1       STR INST.
40122   0100 00 0 40177            TZE   SI1D-1        TO TRY AGAIN.

40123   0760 00 0 00161            SWT   1           WANT A CLOSED LOOP...
40124   0020 00 0 40134            TRA   SI1E        UP-NO-CHECK LOC 00000
40125   0020 00 0 40112            TRA   SI1A-4      DN-YES-REPEAT SAME VALUE.
            ENTRY FOR CONDITION OF FALSE TRAP.

40126   0760 00 0 00161  TRPRT     SWT   1          CLOSED LOOP
40127   0020 00 0 40131            TRA   *+2         UP-NO-PRINT ERROR
40130   0020 00 0 40112            TRA   SI1A-4      DN- YES-REPEAT SAME VALUE.

40131   0074 00 4 00104            TSX   ERROR-1,4
40132   0761 00 0 40106            NOP   SI1
40133   0020 00 0 40177            TRA   SI1D-1     TO STEP TO NEXT INST.
                                WE HAVE AN ERROR---
                                DID WE ALTER S-20 OF LOC 00000...
40134   0500 00 0 00000  SI1E      CLA               LOCATION 00000.
40135   0771 00 0 00017            ARS   15          ELIMINATE
40136   0767 00 0 00017            ALS   15             21-35.
40137   0402 00 0 45122            SUB   INTL1
40140   0100 00 0 40145            TZE   *+5         OK-CK ADDR OF LOC 00000.
40141   0500 00 0 00000            CLA
40142   0560 00 0 45122            LDQ   INTL1
40143   0074 00 4 00104            TSX   ERROR-1,4
40144   0020 00 0 40106            TRA   SI1
    A SI INST ALTERED THE CONTENTS OF S-20 OF LOCATION ZERO.
     XRA INDICATES THE SI INST BEING EXECUTED.
```

```
                                        DID WE ALTER 21-35 OF LOC 00000...

40145  0534 00 2 00000          LXA 0,2        ADDR OF LOC 00000
40146  0754 00 2 00000          PXA 0,2
40147  0100 00 0 40177          TZE SI1D-1     TRY AGAIN.

                                        TRA TO TRPER IF WRONG ADDR STORED.
40150   3 40116 2 40157          TXH TRPER,2,SI1A ABOVE- ERROR-
40151  -3 40115 2 40157          TXL TRPER,2,SI1A-1, BELOW- ERROR-
40152  0560 00 0 45100          LDQ BZERO
40153  0074 00 4 00104          TSX ERROR-1,4
40154  0761 00 0 40106          NOP SI1        FOR DEPR
40155  0020 00 0 40177          TRA SI1D-1     TRY AGAIN.

     A SI INST CAUSED FALSE TRAPPING BY STORING AN ADDR
   IN COLS 21-35 OF LOCATION 00000.

     FOR THE TRAPPING OPERATION TO FUNCTION, THOUGH IN ERROR,
  THE END OPERATION IN I TIME MUST NOT BE FUNCTIONING PROPERLY.
40156  635147255151             BCD 1TRPERR
40157  0560 00 0 45100   TRPER  LDQ BZERO
40160  0074 00 4 00104          TSX ERROR-1,4
40161  0761 00 0 40157          NOP *-2        FOR OPN CODE.
40162  0020 00 0 40177          TRA SI1D-1

     A SI INSTRUCTION CAUSED FALSE TRAPPING BY STORING AN ADDR
   IN COL 21-35 OF LOCATION 00000. THE ADDR STORED IS NOT THE
   ADDR THAT SHOULD HAVE BEEN STORED IN THIS LOCATION.
    ERROR IN STORING ADDR SHOULD HAVE BEEN PREV DETECTED.
          SI INSTRUCTIONS TESTED FOR FALSE TRAPPING
                                                                    XRA
40163  0044 00 0 00000   SIIT   PAI            ELEVEN SI            13
40164  0043 00 0 00000          OAI              INSTRUCTIONS.      12
40165 -0055 00  000000          SIL            ALL ELEVEN           11
40166  0055 00  000000          SIR             ARE ONE CYCLE       10
40167 -0042 00 0 00000          RIA               INSTRUCTIONS.      7
40170  0057 00  000000          RIR                                  6
40171 -0057 00  000000          RIL                                  5
40172  0041 00 0 00000          IIA                                  4
40173  0051 00  000000          IIR                                  3
40174 -0051 00  000000          IIL                                  2
40175 -0046 00 0 00000          PIA                                  1
40176  0000 00 0 00000          HTR            ENTER IF ERROR IN XRA.

40177  2 00001 1 40112          TIX SI1A-4,1,1 LOOP 11 TIMES.
40200  0074 00 4 00106   SI1D   TSX OK,4       CONTINUE TEST.
40201  0020 00 0 40106          TRA SI1        REPEAT TEST.
```

S E C T I O N T H R E E

CHECKING TLQ TO CONDITION THE SI SKIP OR TRA INST

WITH TLQ ASSUMED FUNCTIONAL, A CHECK IS MADE TO SEE IF TLQ WILL CONDITION THE SI SKIP INSTRUCTIONS. INITIAL CONDITIONS ARE SUCH THAT SHOULD TLQ CAUSE A SKIP OR TRA, THIS SKIP OR TRA IS DUE TO A SI INST. TLQ SHOULD NOT TRA.

```
40202  636231026060              BCD 1TSI2
40203  0074 00 4 45152   SI2     TSX  CLEAR,4
40204  0500 00 0 45100           CLA BZERO      ALL ZEROES.
40205  0560 00 0 45101           LDQ BS135      ALL ONES.
40206  0765 00 0 00000           LRS 0          DROP MQ SIGN.
40207  0040 00 0 40212           TLQ *+3        TRA IF MQ LOWER ACC.
40210  0020 00 0 40214           TRA SI2A-1     NORM- CK TO SEE ACC ZERO.
40211  0074 00 2 40215           TSX SI2A,2     WOULD ONLY GET HERE
                                      IF THE SI SKIP INST FUNCTIONED.

40212  0074 00 2 40215           TSX SI2A,2     IN CASE OPER CAUSED TRA.
40213  0074 00 2 40215           TSX SI2A,2     TLQ CAUSED TRA AND SI INST
                                                CAUSED PROG SKIP.
40214  0100 00 0 40220           TZE SI2A+3     ACC SHOULD STILL BE ZERO.

40215  0634 00 2 45135   SI2A    SXA LIES,2     TO PUT TRUE ADDR OF
40216  0535 00 2 45135           LAC LIES,2     LOC INDICATING ERROR.
40217  0074 00 4 00105           TSX ERROR,4
40220  0074 00 4 00106           TSX OK,4       CONTINUE TEST.
40221  0020 00 0 40203           TRA SI2        REPEAT TEST.
```

TLQ EITHER CAUSED THE TIF OR SKIP SI INST TO FUNCTION.
XRB INDICATES THE LOCATION FROM WHICH ERROR WAS DETECTED.

XRB INDICATES ERROR ADDRESS.

TESTING FOR HOT ONES FROM SI REG TO SR
WHEN SI REG IS LOADED WITH ONES - 21-35

TO FURTHER ASSURE THAT ALL ONES ARE LOADED TO SI REG, SIX SI INST AND THREE COMMAND LINES ARE USED.

BEFORE TSXING ON ERROR, THE SI REG IS CLEARED AND CHECKED TO SEE IF ALL HOT ONES HAVE BEEN CLEARED. IF SI COLS ARE NOT CLEARED THE MACHINE SHOULD STOP ON A HPR INSTRUCTION. PUSHING THE START BUTTON SHOULD CAUSE THE MACHINE TO TSX TO PRINT ON PREV ERR.

COLS 21-35 ARE CHECKED FIRST TO FURTHER ELIMINATE POSSIBILITY OF AN ADDRESS MODIFICATION.

```
40222  636231046060              BCD 1TSI4
40223  0074 00 4 45152    SI4    TSX  CLEAR,4
40224  0774 00 1 77777           AXT 32K,1      32K EQ HIGHEST LOC STOR.
40225  0634 00 1 77777           SXA 32K,1      ONES - 21-35
40226  0441 00 0 77777           LDI 32K        ----- LOADING SI REG---
40227  0442 00 0 77777           OSI 32K           COLS 21-35 ----
40230  0600 00 0 77777           STZ 32K        CLEAR LOC
40231 -0754 00 0 00000           PXD            CLEAR ACC
40232  0601 00 0 77777           STO 32K        HOT ONES IN SR TO 32K.

40233  0754 00 1 00000           PXA 0,1        ONES - ACC 21-35.
40234  0044 00 0 00000           PAI            ---- LOADING SI REG
40235  0043 00 0 00000           OAI               COLS 21-35 ----
40236 -0754 00 0 00000           PXD            CLEAR  ACC
40237 -0602 00 0 77777           ORS 32K        --ORING HOT ONES IN SR--
40240  0560 00 0 77777           LDQ 32K        TO MQ FOR TEMP STOR
                                 CLEAR SI REG FOR INVERT INST.
40241 -0754 00 0 00000           PXD            CLEAR ACC
40242  0600 00 0 77777           STZ 32K        CLEAR LOC
40243  0044 00 0 00000           PAI            --CLEARING SI REG,
40244  0441 00 0 77777           LDI 32K              TRYING AGAIN,
40245  0634 00 1 77777           SXA 32K,1      ONES - 21-35
40246  0754 00 1 00000           PXA 0,1        ONES ACC - 21-35
40247 -0042 00 0 00000           RIA                   AGAIN,
40250  0445 00 0 77777           RIS 32K                   AND AGAIN--

40251  0041 00 0 00000           IIA            ---- LOADING SI REG
40252  0440 00  077777          IIS 32K           COLS 21-35.
40253 -0754 00 0 00000           PXD            CLEAR ACC
40254  0600 00 0 77777           STZ 32K        CLEAR LOC
40255 -0600 00 0 77777           STQ 32K           OR HOT ONES IN SR WITH M
40256  0560 00 0 77777           LDQ 32K        BACK TO MQ FOR TEMP STOR.

                                 DID WE GATE ANY ONES OUT OF SI COLS..
40257 -0520 00 0 77777           NZT 32K
40260  0020 00 0 40312           TRA SI4A+1        NO- OK -GO ON.
                                                   YES-ERROR. CLEAR
                                 SI REG BEFORE TSXING TO ERROR, TO
                                 ELIM POSS OF ADDR MODIFICATION.
```

S E C T I O N T H R E E

```
                                        4 SI INST AND 2 COMM LINES ARE USED
                                        IN CLEARING SI REGISTER.
40261   0774 00 1 77777          AXT  32K,1      32K EQ HIGH LOC STOR.
40262   0754 00 1 00000          PXA  0,1           ONES - 21-35.
40263  -0042 00 0 00000          RIA             --RESET 21-35, WE HOPE.--
40264   0600 00 0 77777          STZ  32K        CLEAR STOR
40265  -0500 00 0 77777          CAL  32K        -HOT ONES IN SR TO ACC-
40266   0100 00 0 40307          TZE  SI4A-2     OK-PROCEED ON PREV ERROR.
40267  -0754 00 0 00000          PXD             CLEAR ACC
40270   0044 00 0 00000          PAI                ---TRYING AGAIN,
40271   0600 00 0 77777          STZ  32K        CLEAR LOC
40272  -0500 00 0 77777          CAL  32K        -HOT ONES IN SR TO ACC-
40273   0100 00 0 40307          TZE  SI4A-2     OK-PROCEED ON PREV ERROR.
40274   0634 00 1 77777          SXA  32K,1      ONES - 21-35
40275   0445 00 0 77777          RIS  32K                   AGAIN,
40276   0600 00 0 77777          STZ  32K        CLEAR LOC
40277  -0500 00 0 77777          CAL  32K        -HOT ONES IN SR TO ACC-
40300   0100 00 0 40307          TZE  SI4A-2     OK-PROCEED ON PREV ERROR.
40301   0634 00 1 77777          SXA  32K,1      ONES - 21-35.
40302   0441 00 0 77777          LDI  32K                        AND AGAIN--
40303   0600 00 0 77777          STZ  32K        CLEAR LOC
40304  -0500 00 0 77777          CAL  32K        -HOT ONES IN SR TO ACC-
40305   0100 00 0 40307          TZE  SI4A-2     OK-PROCEED ON PREV ERROR.
40306   0420 00 0 00000          HPR             HOT ONES IN SR THAT WERE
                                        NOT CLEARED BY RESETTING SI REG.
```

NO NEED CONINTUING UNLESS COL 21-35 IS CLEAR. THE BITS IN ERROR ARE DISPLAYED IN ACC P-35. THE MQ S-35 CONTAINS THE HOT BITS FROM SI REG WHEN SI REG IS LOADED WITH ONES.

WITH AT LEAST ONE OF THESE COMMAND LINES FUNCTIONAL, THE FAULT LIES WITHIN THE SI REGISTER LOGIC BLOCKS AND THEIR INPUT AND OUTPUTS.

```
                                        PRINTOUT FOR HOT ONES INDICATION.
40307  -0754 00 0 00000          PXD             CLEAR ACC
40310   0131 00 0 00000          XCA             HOT ONES IN MQ TO ACC
40311   0074 00 4 00105   SI4A   TSX  ERROR,4
40312   0074 00 4 00106          TSX  OK,4       CONTINUE TEST
40313   0020 00 0 40223          TRA  SI4        REPEAT TEST
```

THE ACC P-35 CONTAINS THE HOT ONES FROM SI REG TO SR, WHEN THE SI REG IS LOADED WITH ONES. CHECK THE OUTPUT OF THE SI REG, 2.06 PAGES

THE CONTENTS OF THE INDICATORS INDICATES WHAT WAS STORED BY USE OF THE STI INST WHICH HAS NOT AS YET BEEN CHECKED.

TESTING FOR HOT ONES FROM SI REG TO SR
WHEN SI REG IS LOADED WITH ALL ONES

TO FURTHER ASSURE THAT ALL ONES ARE LOADED TO SI REG, SIX SI INST AND THREE COMMAND LINES ARE USED. THIS ROUTINE ASSUMES THAT ADDR MODIFICATION IS NOT POSSIBLE.

BEFORE TSXING ON ERROR. THE SI REG IS CLEARED AND CHECKED TO SEE IF ALL HOT ONES HAVE BEEN CLEARED. FAILURE TO CLEAR WILL CAUSE MACHINE TO PRINTOUT WITH ERRORS IN ACC BEFORE TSXING TO PRINT ON PREV ERROR.

```
40314  636231056060            BCD 1TSI5
40315  0074 00 4 45152   SI5   TSX  CLEAR,4
40316  0074 00 2 40346         TSX SICL1,2   CLEAR SI REG.

40317  0600 00 0 45135         STZ LIES      INITIALIZE.
40320  0774 00 1 00004         AXT 4,1       LOAD XRA FOR XEC INST.
40321 -0500 00 0 45101         CAL BS135     ONES- ACC P-35.
40322  0522 00 1 45132         XEC LOAD+4,1  LOAD WITH FOUR SI INST.
40323 -0754 00 0 00000         PXD           CLEAR ACC
40324 -0602 00 0 45135         ORS LIES      HOT ONES IN SR TO STOR.
40325  2 00001 1 40321         TIX *-4,1,1
40326  0074 00 2 40346         TSX SICL1,2   CLEAR SI REG.

40327  0440 00  045101         IIS BS135
40330 -0754 00 0 00000         PXD            CLEAR ACC.
40331 -0602 00 0 45135         ORS LIES      HOT ONES IN SR TO STOR.
40332  0074 00 2 40346         TSX SICL1,2   CLEAR SI REG

40333 -0500 00 0 45101         CAL BS135     ONES- ACC P-35.
40334  0041 00 0 00000         IIA
40335 -0754 00 0 00000         PXD           CLEAR ACC.
40336 -0602 00 0 45135         ORS LIES      HOT ONES IN SR TO STOR.

40337 -0520 00 0 45135         NZT LIES
                                   DO WE HAVE ANY HOT ONES...
40340  0020 00 0 40345         TRA  *+5      NO-OK- GO ON.
40341  0500 00 0 45135         CLA LIES
40342  0560 00 0 45100         LDQ BZERO
40343  0074 00 4 00104         TSX  ERROR-1,4
40344  0020 00 0 40315         TRA  SI5
40345  0020 00 0 40376         TRA  SI7-3
```

THE SI REG OUTPUT IS PUTTING HOT ONES TO SR. THE ACC S-35 CONTAIN THE HOT ONES THAT WERE PRESENT.
THE CONTENTS OF THE INDICATORS INDICATES WHAT WAS STORED BY USE OF THE STI INST WHICH HAS NOT AS YET BEEN CHECKED.

S E C T I O N T H R E E

SUBROUTINE - SI CLEAR 1

USED TO FURTHER ASSURE CLEARING OF SI REG UNTIL THE LDI INST
IS CHECKED. SUBROUTINE USES FOUR SI INST AND TWO COMMAND LINES.
SUBROUTINE USED IN CONJUNTION WITH TEST FOR CHECKING SR HOT ONES.

```
40346 -0500 00 0 45101   SICL1 CAL BS135      ONES - P-35.
40347 -0042 00 0 00000         RIA            CLEARING SI REG 0-35--
40350 -0500 00 0 45100         CAL BZERO      HOT ONES IN SR TO ACC...
40351  0100 00 2 00001         TZE 1,2        CLEARED- OK -RETURN.

40352  0445 00 0 45101         RIS BS135      ---- TRYING AGAIN,--
40353 -0500 00 0 45100         CAL BZERO      HOT ONES IN SR TO ACC...
40354  0100 00 2 00001         TZE 1,2        CLEARED- OK -RETURN.

40355 -0754 00 0 00000         PXD            CLEAR ACC
40356  0044 00 0 00000         PAI            --AGAIN,--
40357 -0500 00 0 45100         CAL BZERO      HOT ONES IN SR TO ACC...
40360  0100 00 2 00001         TZE 1,2        CLEARED- OK -RETURN.

40361  0441 00 0 45100         LDI BZERO      -- AND AGAIN.---
40362 -0500 00 0 45100         CAL BZERO      HOT ONES IN SR TO ACC...
40363  0100 00 2 00001         TZE 1,2        CLEARED- OK -RETURN.

                                  ALL HOT ONES NOT CLEARED--
40364  0634 00 2 45143         SXA LIES+6,2   SAVE XRB
40365  0535 00 2 45143         LAC LIES+6,2   GET 2S COMPLEMENT TO
40366  0634 00 2 45144         SXA LIES+7,2      GIVE TRUE ADDRESS.
40367  0560 00 0 45144         LDQ LIES+7     ERROR ADDR TO MQ-PRINTOUT
40370  0534 00 2 45143         LXA LIES+6,2
40371  0020 00 0 40373         TRA *+2        JUMP OVER.
40372  623123435101            BCD 1SICLR1
40373  0074 00 4 00104         TSX ERROR-1,4
40374  0761 00 0 40373         NOP *-1
40375  0020 00 2 00001         TRA 1,2
```

WITH THE USE OF FOUR SI INST AND TWO COMMAND LINES, THE SI REG WAS
NOT CLEARED TO CLEAR HOT ONES FROM SI REG TO SR.
THE ACC P-35 CONTAINS THE HOT ONES THAT WERE NOT CLEARED.
THE ADDR OF MQ CONTAINS THE ADDRESS OF TEST USING SICL1.

```
40376  0074 00 4 00106         TSX  OK,4
40377  0020 00 0 40315         TRA  SI5
```

ASSUMING THAT NO HOT ONES FROM SI REG TO SR IS PRESENT WHEN SI REG IS LOADED, A CHECK IS NOW MADE TO DETERMINE WHETHER THE SET SI TO SR COMMAND LINE WILL GATE SOMETHING FROM THE SI REG TO SR. SIX SI INST WILL BE USED TO FURTHER INSURE POSSIBILITY OF LOADING SI REG WITH ONES.

TESTING-SET SI TO SR COMMAND LINE 2.12.13

```
40400  636231076060              BCD 1TSI7
40401  0074 00 4 45152   SI7     TSX  CLEAR,4
40402  0774 00 1 00006           AXT 6,1        LOAD XRA FOR XEC.
40403 -0500 00 0 45101           CAL BS135
40404  0522 00 1 45134           XEC LOAD+6,1   XEC SIX SI INST.
40405  0604 00 0 45135           STI LIES       IND TO STOR FOR CHECK
40406 -0754 00 0 00000           PXD            CLEAR  ACC
40407 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK
40410 -0602 00 0 45137           ORS LIES+2
40411 -0500 00 0 45135           CAL LIES
40412 -0602 00 0 45136           ORS LIES+1
40413  2 00001 1 40403           TIX SI7+2,1,1
                                     DID WE STORE*STI LIES* INSTEAD
                                     OF SOMETHING FROM SI REG...
40414  0500 00 0 45136           CLA LIES+1
40415  0402 00 0 40405           SUB SI7+4      LOC OF *STI LIES*
40416 -0100 00 0 40427           TNZ SI7A       NO-SOMETHING WAS GATED.
                                                YES- *STI LIES* WAS STORED


40417  0500 00 0 45137           CLA LIES+2
40420  0402 00 0 40407           SUB SI7+6      LOC OF *PIA*
40421 -0100 00 0 40427           TNZ SI7A       PIA INST GATED SOMETHING.
40422  0500 00 0 45136           CLA LIES+1     STOR LOC FOR STI INST
40423  0560 00 0 45137           LDQ LIES+2     STOR LOC FOR PIA INST
40424  0074 00 4 00104           TSX  ERROR-1,4
40425  0020 00 0 40401           TRA  SI7
40426  0020 00 0 40433           TRA  SI7A+4
```

BOTH STI AND PIA FAILED TO GATE THE TRUE IND TO SR, 2.12.13. THE CONT OF SR WERE NOT CLEARED BY THESE TWO INSTRUCTIONS.

```
                                        BOTH STI AND PIA GATED SOMETHING
                                        TO SR. WAS IT ZEROES...
40427 -0500 00 0 45136   SI7A  CAL LIES+1
40430 -0501 00 0 45137         ORA LIES+2
                                    DID WE GATE ONLY ZEROES...
40431 -0100 00 0 40433         TNZ *+2        NO-  OK  -GO ON
40432  0074 00 4 00105         TSX ERROR,4    YES-ERROR
40433  0074 00 4 00106         TSX OK,4       CONTINUE TEST.
40434  0020 00 0 40401         TRA SI7        REPEAT TEST .
```

BOTH STI AND PIA CLEARED SR BUT GATED ZEROES INTO SR.
EITHER SI REG WAS NOT LOADED OR SI REG WAS NOT GATED TO SR.

TESTING STI TO GATE SI REG TO SR

```
40435  626331606060            BCD 1STI       INST +0604
40436  0074 00 4 45152   SI8   TSX  CLEAR,4
40437 -0500 00 0 45101         CAL BS135      ONES - P-35
40440 -0042 00 0 00000         RIA            --CLEARING
40441  0441 00 0 45100         LDI BZERO                SI
40442  0445 00 0 45101         RIS BS135                   REG--
40443  0604 00 0 45135         STI LIES       IND TO STOR FOR CHECK.
40444  0500 00 0 45135         CLA LIES       DID WE STORE*STI LIES*
                                              INSTEAD CONT OF SI REG
40445  0402 00 0 40443         SUB *-2
40446 -0100 00 0 40451         TNZ *+3        NO - STI GATED SOMETHING
                                              FROM SI REG TO SR.
40447  0500 00 0 45135         CLA LIES
40450  0074 00 4 00105         TSX ERROR,4
40451  0074 00 4 00106         TSX OK,4       CONTINUE TEST
40452  0020 00 0 40436         TRA SI8        REPEAT TEST.
```

STI FAILED TO GATE THE SI REG TO SR. THE ACC S-35 CONTAINS
THE INSTRUCTION WORD STI LIES .

TESTING PIA TO CONDITION ADD TO ACC COMMAND LINE 2.12.31.

```
40453  473121606060              BCD 1PIA
40454  0074 00 4 45152   SI9     TSX  CLEAR,4
40455  0500 00 0 45110           CLA P52S       BIT PATTERN 101 010
40456 -0046 00 0 00000           PIA
40457  0602 00 0 45135           SLW LIES
40460  0500 00 0 45135           CLA LIES
40461  0402 00 0 45110           SUB P52S
                                     DID WE ALTER CONT OF ACC...
40462 -0100 00 0 40465           TNZ *+3        YES-  OK  -GO ON.
40463  0500 00 0 45135           CLA LIES       NO-  ERROR
40464  0074 00 4 00105           TSX ERROR,4
40465  0074 00 4 00106           TSX OK,4       CONTINUE TEST
40466  0020 00 0 40454           TRA SI9        REPEAT TEST
```

PIA FAILED TO CONDITION THE ADD TO ACC COMM LINE TO ALTER THE CONTENTS OF THE ACC.

SIX SI INST ARE USED TO FURTHER ASSURE THAT SI REG CAN BE LOADED.

TESTING PIA TO CONDITION SR TO ADD COMMAND LINE 2.12.15.
ADD TO ACC COMM LINE SHOULD BE FUNCT.

```
40467  473121606060              BCD 1PIA
40470  0074 00 4 45152   SI10    TSX  CLEAR,4
40471  0774 00 1 00006           AXT 6,1        LOADING XRA FOR XEC
40472 -0500 00 0 45101           CAL BS135      ALL ONES
40473  0522 00 1 45134           XEC LOAD+6,1
40474 -0754 00 0 00000           PXD            CLEAR  ACC
40475 -0046 00 0 00000           PIA
40476 -0602 00 0 45135           ORS LIES
40477  2 00001 1 40472           TIX SI10+2,1,1  LOOP SIX TIMES.
40500  0520 00 0 45135           ZET LIES
                                     DID WE PUT SOMETHING IN ACC FROM SR..
40501  0020 00 0 40504           TRA *+3        YES-  OK  -GO ON
40502  0500 00 0 45135           CLA LIES       NO-  ERROR
40503  0074 00 4 00105           TSX ERROR,4
40504  0074 00 4 00106           TSX OK,4       CONTINUE TEST
40505  0020 00 0 40470           TRA SI10       REPEAT TEST
```

PIA FAILED TO CONDITION THE SR TO ADD COMM LINE TO GATE ANY ONES TO ACC.

TESTING PIA TO CONDITION SI TO SR COMMAND LINE 2.12.13
SR TO ADD AND ADD TO ACC COMMAND LINES SHOULD BE FUNCTIONAL.

```
40506  473121606060
40507   0074 00 4 45152   SI11  BCD 1PIA
40510   0774 00 1 00006         TSX  CLEAR,4
40511  -0500 00 0 45101         AXT 6,1          LOADING XRA FOR XEC
40512   0522 00 1 45134         CAL BS135        ALL ONES
40513  -0754 00 0 00000         XEC LOAD+6,1     XEC SIX SI INST
40514  -0046 00 0 00000         PXD              CLEAR  ACC
40515  -0602 00 0 45135         PIA
40516   2 00001 1 40511         ORS LIES
40517   0500 00 0 45135         TIX SI11+2,1,1
40520   0402 00 0 40514         CLA LIES
                                SUB SI11+5       LOC OF *PIA*
                                    DID WE ALTER CONT OF SR...
40521  -0100 00 0 40524         TNZ *+3          YES-  OK  -GO ON
40522   0500 00 0 45135         CLA LIES         NO-  ERROR
40523   0074 00 4 00105         TSX ERROR,4
40524   0074 00 4 00106         TSX OK,4         CONTINUE TEST
40525   0020 00 0 40507         TRA SI11         REPEAT TEST
```

PIA FAILED TO CONDITION THE SI TO SR COMM LINE TO ALTER THE CONTENTS OF SR WHICH IS GATED TO ACC.

TESTING TRUE IND TO SR COMMAND LINE FOR COMPLETE FUNCTION

KNOWING THAT STI AND PIA WILL GATE SOMETHING FROM SI REG TO SR, A CHECK WILL BE MADE TO SEE IF TRUE IND TO SR IS COMPLETELY FUNCTIONAL. SIX SI INST WILL BE USED TO FURTHER ASSURE THAT ALL ONES CAN BE LOADED INTO SI REG.

```
40526  636231010260
40527   0074 00 4 45152   SI12  BCD 1TSI12
40530   0774 00 1 00006         TSX  CLEAR,4
40531  -0500 00 0 45101         AXT 6,1          LOAD XRA FOR XEC
40532   0522 00 1 45134         CAL BS135        ALL ONES
40533  -0754 00 0 00000         XEC LOAD+6,1     XEC SIX SI INST
40534  -0046 00 0 00000         PXD              CLEAR  ACC
40535  -0602 00 0 45135         PIA
40536   2 00001 1 40531         ORS LIES
40537   0500 00 0 45135         TIX SI12+2,1,1
40540   0402 00 0 45101         CLA LIES
                                SUB BS135
                                    DID WE GATE ALL ONES FROM SI REG...
40541   0100 00 0 40545         TZE *+4          YES-  OK  -GO ON.
40542   0500 00 0 45135         CLA LIES
40543   0560 00 0 45101         LDQ BS135
40544   0074 00 4 00105         TSX ERROR,4
40545   0074 00 4 00106         TSX OK,4         CONTINUE TEST
40546   0020 00 0 40527         TRA SI12         REPEAT TEST
```

THE TRUE IND TO SR COMMAND LINE DID NOT COMPLETELY GATE THE SI REG TO SR, ASSUMING THAT ALL SI REG COLS COULD BE LOADED BY AT LEAST ONE OF THE SIX SI INST.

THE ACC S-35 CONTAIN THE ONES THAT WERE GATED FROM SI REG. THE IND PRINTOUT CONTAINS ONLY THE CONDITION OF THE LAST XEC INST. WE SHOULD BE ABLE TO ASSUME THAT ALL ONES CAN BE SET OUT OF SI REG, THOUGH ALL ONES MAY NOT BE ABLE TO BE LOADED INTO SI REG.

```
                TESTING STI WITH SI REG SET TO ZERO
40547   636231010560                BCD 1TSI15
40550   0074 00 4 45152     SI15    TSX  CLEAR,4
40551  -0500 00 0 45101             CAL BS135       ONES - ACC P-35
40552  -0042 00 0 00000             RIA
40553   0074 00 2 40564             TSX SI15A,2     CHECK RESULT
40554   0445 00 0 45101             RIS BS135
40555   0074 00 2 40564             TSX SI15A,2     CHECK RESULT
40556  -0754 00 0 00000             PXD             CLEAR ACC
40557   0044 00 0 00000             PAI
40560   0074 00 2 40564             TSX SI15A,2     CHECK RESULT
40561   0441 00 0 45100             LDI BZERO
40562   0074 00 2 40564             TSX SI15A,2     CHECK RESULT
40563   0020 00 0 40572             TRA *+7         OK  -  GO ON.
40564   0604 00 0 45135     SI15A   STI LIES        IND TO STOR FOR CHECK
40565   0500 00 0 45135             CLA LIES
40566   0402 00 0 40564             SUB *-2
                                        DID WE GATE CONT OF SR BEFORE SI-SR
40567  -0100 00 2 00001             TNZ 1,2         RETURN TO TEST
40570   0500 00 0 45135             CLA LIES
40571   0074 00 4 00105             TSX ERROR,4
40572   0074 00 4 00106             TSX OK,4        CONTINUE TEST
40573   0020 00 0 40550             TRA SI15        REPEAT TEST


                TESTING PIA WITH SI REG SET TO ZERO
40574   636231010522                BCD 1TSI15B
40575   0074 00 4 45152     SI15B   TSX  CLEAR,4
40576   0500 00 0 45101             CLA BS135       ONES - ACC P-35
40577  -0042 00 0 00000             RIA
40600   0074 00 2 40611             TSX SI15C,2     CHECK RESULT
40601   0445 00 0 45101             RIS BS135
40602   0074 00 2 40611             TSX SI15C,2     CHECK RESULT
40603  -0754 00 0 00000             PXD             CLEAR ACC
40604   0044 00 0 00000             PAI
40605   0074 00 2 40611             TSX SI15C,2     CHECK RESULT
40606   0441 00 0 45100             LDI BZERO
40607   0074 00 2 40611             TSX SI15C,2     CHECK RESULT
40610   0020 00 0 40620             TRA *+8         OK  -  GO ON
40611  -0046 00 0 00000     SI15C   PIA             IND TO STOR FOR CHECK
40612   0602 00 0 45135             SLW LIES
40613   0500 00 0 45135             CLA LIES
40614   0402 00 0 40611             SUB *-3
                                        DID WE GATE CONT OF SR BEFORE SI-SR
40615  -0100 00 2 00001             TNZ 1,2         RETURN TO TEST
40616   0500 00 0 45135             CLA LIES
40617   0074 00 4 00105             TSX ERROR,4
40620   0074 00 4 00106             TSX OK,4        CONTINUE TEST
40621   0020 00 0 40575             TRA SI15B       REPEAT TEST
    WITH SI COLS SET TO ZERO, PIA STORED THE CONT OF SR BEFORE SI-SR
```

S E C T I O N T H R E E

TESTING SI REG TO BE COMPLETELY LOADED WITH ALL ONES

SIX SI INST WHICH USE TWO COMM LINES ARE USED IN LOADING SI REG. TRUE IND TO SR COMM LINE SHOULD BE FUNCTIONAL.

```
40622   636231010660              BCD 1TSI16
40623   0074 00 4 45152    SI16   TSX  CLEAR,4
40624   0774 00 1 00006           AXT 6,1        LOADING XRA FOR XEC INST
40625  -0500 00 0 45101           CAL BS135

40626   0522 00 1 45134           XEC LOAD+6,1   XEC SIX SI INST

40627  -0046 00 0 00000           PIA
40630  -0602 00 0 45135           ORS LIES
40631   2 00001 1 40625           TIX SI16+2,1,1

40632  -0500 00 0 45135           CAL LIES
40633   0760 00 0 00006           COM
40634   0767 00 0 00001           ALS 1          DROP EXISTING Q BIT.
                                      DID WE SET ALL SI COLS...
40635   0100 00 0 40640           TZE *+3        YES-  OK  -GO ON
40636   0500 00 0 45135           CLA LIES       NO-  ERROR
40637   0074 00 4 00105           TSX ERROR,4
40640   0074 00 4 00106           TSX OK,4       CONTINUE TEST
40641   0020 00 0 40623           TRA SI16       REPEAT TEST
```

USING TWO DIFFERENT COMMAND LINES AND SIX SI INST, THE SI REG WAS NOT COMPLETELY SET TO ALL ONES.

HAVING BEEN PREVIOUSLY CHECKED, THE TRUE IND TO SR COMMAND LINE SHOULD BE FUNCTIONAL. THIS IS ALSO TRUE FOR PIA.

THE CONT OF ACC P-35 INDICATE SI REG COLS NOT LOADED. THE CONT OF IND PRINTOUT INDICATES THE SI REG COLS LOADED. FOR THOSE NOT LOADED, CHECK RESPECTIVE SI COLS. 2.06 PAGES

TESTING SI REG TO BE CLEARED AFTER BEING COMPLETELY LOADED

SIX SI INST AND TWO COMMAND LINES ARE USED FOR LOADING SI REG
FOUR SI INST AND TWO COMMAND LINES ARE USED IN CLEARING SI.

```
40642  636231010760              BCD 1TSI17
40643  0074 00 4 45152    SI17   TSX  CLEAR,4
40644  0441 00 0 45101           LDI BS135
40645  0442 00 0 45101           OSI BS135
40646  0074 00 2 40724           TSX SICL2,2

40647 -0500 00 0 45101           CAL BS135
40650  0044 00 0 00000           PAI
40651  0043 00 0 00000           OAI
40652  0074 00 2 40724           TSX SICL2,2

40653 -0500 00 0 45101           CAL BS135
40654  0041 00 0 00000           IIA
40655  0074 00 2 40724           TSX SICL2,2

40656  0440 00  045101           IIS BS135
40657  0074 00 2 40724           TSX SICL2,2


                                     DID WE CLEAR SI REG EACH TIME...
40660 -0520 00 0 45135           NZT LIES
40661  0020 00 0 40664           TRA *+3        YES-  OK  -GO ON
40662  0500 00 0 45135           CLA LIES       NO-  ERROR
40663  0074 00 4 00105           TSX ERROR,4
40664  0074 00 4 00106           TSX OK,4       CONTINUE TEST
40665  0020 00 0 40643           TRA SI17       REPEAT TEST
```

USING SIX SI INST TO FURTHER ASSURE THAT EACH SI COL IS LOADED AND FOUR SI INST AND TWO COMMAND LINES TO CLEAR SI REG, THE SI REG COLS WERE NOT ALL COMPLETELY CLEARED.

THE CONT OF ACC INDICATES THE COLS IN ERROR. THE CONT OF IND INDICATE THE CONDITION FOR IIS ONLY.

FOR THOSE NOT CLEARED, CHECK RESPECTIVE SI COLS. 2.06 PAGES

IF THE RESPECTIVE SI COLS ARE COMPLETELY FUNCTIONAL, THE PROGRAM CAN BE CONTINUED. ERRORS IN THE EXECUTION OR COMMAND LINES SHOULD BE INDICATED BY THE ROUTINES OF THE INDIVIDUAL SI INST.

S E C T I O N T H R E E

CHECKING TLQ TO CONDITION THE ONE CYCLE SI INST.

```
40666  636231011060            BCD 1TSI18
40667  0074 00 4 45152   SI18  TSX  CLEAR,4
40670  0500 00 0 45110         CLA P52S       ALT ONES - 101 010
40671  0560 00 0 45101         LDQ BS135      ALL ONES-
40672  0441 00 0 45105         LDI P07S       INST AS YET NOT BEEN TESTED
40673  0040 00 0 40674         TLQ *+1
40674  0761 00 0 00000         NOP            JUST IN CASE OF
40675  0761 00 0 00000         NOP              A SKIP OR TRA.
40676  0604 00 0 45135         STI LIES
40677  0500 00 0 45135         CLA LIES
40700  0402 00 0 45105         SUB P07S       ALT  000  111.
40701  0100 00 0 40723         TZE  SI18A+7   SI NOT ALTERED GO ON .
                                  WAS ACC PUT IN SI REG...
40702  0500 00 0 45135         CLA LIES
40703  0402 00 0 45110         SUB P52S
40704  0100 00 0 40714   SI18C TZE SI18A      YES-  ERROR.
                                  WAS RESET SI LINE CONDITIONED..
40705  0500 00 0 45135         CLA LIES
40706  0402 00 0 45104         SUB P05S       BIT PATT   000 101
40707  0100 00 0 40716   SI18D TZE SI18A+2    YES-  ERROR
                                  WAS INVERT SI LINE CONDITIONED..
40710  0500 00 0 45135         CLA LIES
40711  0402 00 0 45111         SUB P55S       BIT PATT  101 101.
40712  0100 00 0 40720   SI18E TZE SI18A+4    YES-  ERROR.
40713  0020 00 0 40723         TRA  SI18A+7     GO TO NEXT ROUTINE

                                  PUT ERROR LOCATION IN XRB.
40714  0774 00 2 40704   SI18A AXT SI18C,2
40715  0020 00 0 40721         TRA *+4
40716  0774 00 2 40707         AXT SI18D,2
40717  0020 00 0 40721         TRA *+2
40720  0774 00 2 40712         AXT SI18E,2
40721  0074 00 4 00104         TSX  ERROR-1,4
40722  0020 00 0 40667         TRA  SI18
40723  0020 00 0 40756         TRA  SI20-3
```

TLQ CONDITIONED ONE OF THE SI ONE CYCLE INST TO ALTER CONTENTS OF SI REG.

SUBROUTINE USED TO CLEAR SI REG BEFORE LDI BZERO IS CHECKED.
FOUR SI INST AND TWO COMM LINES ARE USED TO FURTHER
ASSURE THAT ALL SI COLS CAN BE CLEARED.

```
40724  0500 00 0 45101   SICL2 CLA BS135      ONES- ACC P-35
40725 -0042 00 0 00000         RIA
40726 -0046 00 0 00000         PIA            IND TO ACC FOR CHECK
40727  0100 00 2 00001         TZE 1,2        RETURN

40730 -0754 00 0 00000         PXD            CLEAR ACC
40731  0044 00 0 00000         PAI
40732 -0046 00 0 00000         PIA            IND TO ACC FOR CHECK
40733  0100 00 2 00001         TZE 1,2        RETURN

40734  0445 00 0 45101         RIS BS135
40735 -0046 00 0 00000         PIA            IND TO ACC FOR CHECK.
40736  0100 00 2 00001         TZE 1,2        RETURN

40737  0441 00 0 45100         LDI BZERO
40740 -0046 00 0 00000         PIA            IND TO ACC FOR CHECK
40741  0100 00 2 00001         TZE 1,2

40742  0602 00 0 45135         SLW LIES
40743  0634 00 2 45143         SXA LIES+6,2   SAVE XRB
40744  0535 00 2 45143         LAC LIES+6,2   GET 2S COMPLEMENT TO
40745  0634 00 2 45144         SXA LIES+7,2      GIVE TRUE ADDRESS.
40746  0500 00 0 45135         CLA LIES
40747  0560 00 0 45144         LDQ LIES+7     ERROR ADDR TO MQ
40750  0534 00 2 45143         LXA LIES+6,2   RESET XRB
40751  0020 00 0 40753         TRA *+2
40752  623123435102            BCD 1SICLR2
40753  0074 00 4 00104         TSX ERROR-1,4
40754  0761 00 0 40753         NOP *-1
40755  0020 00 2 00001         TRA 1,2
```

WITH THE USE OF FOUR SI INST AND TWO COMM LINES, THE SI REG WAS NOT FULLY CLEARED.

ACC S-35 CONTAINS THE SI COLS THAT WERE NOT CLEARED.
MQ 21-35 CONTAINS THE ADDRESS OF TEST USING SICL2.
WITH AT LEAST ONE OF THESE COMM LINES FUNCTIONAL, THE FAULT LIES WITHIN THE SI REG COLS -- 2.06 PAGES.

```
40756  0074 00 4 00106         TSX  OK,4
40757  0020 00 0 40667         TRA  SI18
```

S E C T I O N T H R E E

BEGIN TESTING OF SI INST AND COMMAND LINES

FOR THE FOLLOWING TESTS---
- A- EACH SI REG COL SHOULD BE ABLE TO BE LOADED.
- B- EACH SI REG COL SHOULD BE ABLE TO BE CLEARED.
- C- EACH SI REG COL OUTPUT SHOULD BE ABLE TO BE GATED TO SR BY SI INST PIA OR STI.
- D- BOTH PIA AND STI SHOULD BE COMPLETELY FUNCTIONAL.

IN THE FOLLOWING TESTS---
- 1- THE COMMAND LINE WILL BE TESTED FOR OPERATION, USING ALL INST USING THAT SUCH COMMAND, EXCEPT THE RT AND LT HALF SI INSTRUCTIONS.
- 2- THEN THE INDIVIDUAL EXECUTION LINES TO THE ASSUMED FUNCTIONAL COMM LINE IS TESTED FOR OPER.

TESTING SET SI COMMAND LINES) 2.12.64

```
40760  636231020060            BCD 1TSI20
40761  0074 00 4 45152   SI20  TSX  CLEAR,4
40762  0074 00 2 40724         TSX SICL2,2
40763  0774 00 1 00004         AXT 4,1        LOADING XRA FOR XEC INST.
40764 -0500 00 0 45101         CAL BS135
40765  0522 00 1 45132         XEC LOAD+4,1   XEC FOUR SI INST
40766 -0046 00 0 00000         PIA
40767 -0602 00 0 45135         ORS LIES
40770  2 00001 1 40764         TIX SI20+3,1,1
40771 -0500 00 0 45135         CAL LIES
40772  0760 00 0 00006         COM
40773  0767 00 0 00001         ALS 1          DROP EXISTING Q BIT.
                                DID WE SET ALL SI REG COLS...
40774  0100 00 0 40777         TZE *+3        YES-  OK  -GO ON
40775  0500 00 0 45135         CLA LIES       NO-  ERROR
40776  0074 00 4 00105         TSX ERROR,4
40777  0074 00 4 00106         TSX OK,4       CONTINUE TEST
41000  0020 00 0 40761         TRA SI20       REPEAT TEST
```

USING ITS FOUR INPUTS. THE SET SI COMMAND LINES FAILED TO SET ALL ONES INTO SI REG.

TESTING LDI TO CONDITION SI SET COMMAND LINES. 2.12.64

```
41001  432431606060            BCD 1LDI
41002  0074 00 4 45152   SI21  TSX  CLEAR,4
41003  0074 00 2 40724         TSX SICL2,2
41004  0560 00 0 45101         LDQ BS135      CORR CONT OF SI REG..
41005  0441 00 0 45101         LDI BS135      ALL ONES
41006 -0046 00 0 00000         PIA
41007  0602 00 0 45135         SLW LIES
41010  0760 00 0 00006         COM
41011  0767 00 0 00001         ALS 1          DROP EXISTING Q BIT
                                DID WE LOAD ALL ONES...
41012  0100 00 0 41015         TZE *+3        YES-  OK  -GO ON
41013  0500 00 0 45135         CLA LIES       NO-  ERROR
41014  0074 00 4 00105         TSX ERROR,4
41015  0074 00 4 00106         TSX OK,4       CONTINUE TEST
41016  0020 00 0 41002         TRA SI21       REPEAT TEST
```

LDI FAILED TO CONDITION THE SET SI COMMAND LINES TO SET ALL ONES INTO SI REG. 2.12.63.

TESTING THE ELECTRONIC RESET OF SI COMMAND LINE,2.12.64 .

```
41017  636231020260              BCD 1TSI22
41020  0074 00 4 45152    SI22   TSX  CLEAR,4

41021  0441 00 0 45101           LDI BS135      LOAD SI REG
41022 -0754 00 0 00000           PXD            CLEAR  ACC
41023  0044 00 0 00000           PAI            CLEAR SI REG...
41024  0604 00 0 45135           STI LIES


41025  0441 00 0 45101           LDI BS135      LOAD SI REG ALL ONES.
41026  0441 00 0 45100           LDI BZERO      CLEAR SI REG...
41027 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK
41030  0604 00 0 45136           STI LIES+1


41031 -0340 00 0 45101           LAS BS135      COMPARING LDI ZERO-
                                    DID WE CLEAR ANY OF THE SI COLS...
41032  0020 00 0 41034           TRA *+2        YES -
41033  0020 00 0 41035           TRA *+2        NO - TEST PAI
41034  0020 00 0 41045           TRA SI22A      YES -  OK  - GO ON

41035 -0500 00 0 45136           CAL LIES+1
41036 -0340 00 0 45101           LAS BS135      COMPARING PAI - ACC ZERO-
                                    DID WE CLEAR ANY OF THE SI COLS...
41037  0020 00 0 41041           TRA *+2        YES-
41040  0020 00 0 41042           TRA *+2        NO -  ERROR
41041  0020 00 0 41045           TRA SI22A      YES-  OK  -GO ON

41042  0500 00 0 45135           CLA LIES
41043  0560 00 0 45136           LDQ LIES+1
41044  0074 00 4 00105           TSX ERROR,4
41045  0074 00 4 00106    SI22A  TSX OK,4
41046  0020 00 0 41020           TRA SI22
```

LDI OR PAI INST FAILED TO CONDITION THE ELECTRONIC RESET OF SI COMMAND LINE. 2.12.64.

THE ACC S-35 CONTAINS RESULT OF PAI INST.
THE MQ S-35 CONTAINS RESULT OF LDI INST.
BOTH REGISTERS SHOULD BE ZERO.

TESTING LDI TO CONDITION THE ELECTRONIC RESET OF SI
COMMAND LINE, 2.12.64.

```
41047  432431606060              BCD 1LDI
41050  0074 00 4 45152   SI23    TSX  CLEAR,4
41051  0441 00 0 45101            LDI BS135      LOAD SI REG
41052  0441 00 0 45100            LDI BZERO      CLEARING SI REG.
41053  0604 00 0 45135            STI LIES
41054 -0520 00 0 45135            NZT LIES       IS CONT LIES ZERO...
41055  0020 00 0 41066            TRA SI23A+1    YES- OK -GO ON.
41056  0500 00 0 41052            CLA SI23+2     NO- ERROR. LOC *LDI BZERO*
                                      ELIM TIMING PULSE ERROR POSS.
41057  0340 00 0 45135            CAS LIES
41060  0020 00 0 41062            TRA *+2        ERROR
41061  0020 00 0 41065            TRA SI23A      ELECT RESET OK
41062  0074 00 4 00104            TSX  ERROR-1,4
41063  0020 00 0 41050            TRA SI23       REPEAT TEST
41064  0020 00 0 41066            TRA  SI23A+1     CONTINUE TEST
```

LDI FAILED TO CONDITION THE ELECTRONIC RESET OF SI COMMAND LINE
TO COMPLETELY CLEAR ALL SI REG COLS.

THE ACC S-35 AND IND INDICATE THE SI REG COLS THAT WERE NOT
CLEARED.

```
41065  0074 00 4 00105   SI23A TSX ERROR,4
41066  0074 00 4 00106         TSX OK,4       CONTINUE TEST
41067  0020 00 0 41050         TRA SI23       REPEAT TEST
```

TESTING PAI TO CONDITION SI SET COMMAND LINES. 2.12.64

```
41070  472131606060              BCD 1PAI
41071  0074 00 4 45152   SI24    TSX  CLEAR,4
41072  0441 00 0 45100           LDI BZERO      CLEAR SI REG
41073 -0500 00 0 45101           CAL BS135
41074  0044 00 0 00000           PAI
41075  0604 00 0 45135           STI LIES       IND TO STOR FOR CHECK.
41076  0520 00 0 45135           ZET LIES
                                     DID WE PUT ANYTHING IN SI REG...
41077  0020 00 0 41102           TRA *+3        YES- OK -GO ON
41100  0500 00 0 45135           CLA LIES       NO-  ERROR
41101  0074 00 4 00105           TSX ERROR,4
41102  0074 00 4 00106           TSX OK,4       CONTINUE TEST.
41103  0020 00 0 41071           TRA SI24       REPEAT TEST.
```

ASSUMING THAT LDI CLEARED SI REG, THE PAI INST FAILED TO CONDITION THE +N SET SI LINE TO GATE SOMETHING TO SI REG.

TESTING PAI TO CONDITION THE AC TO SR COMMAND LINE,2.12.02

```
41104  472131606060              BCD 1PAI
41105  0074 00 4 45152   SI25    TSX  CLEAR,4
41106  0441 00 0 45100           LDI BZERO      CLEAR SI REG...
41107  0560 00 0 45101           LDQ BS135      CORR CONT OF SI REG..
41110 -0500 00 0 45101           CAL BS135
41111  0044 00 0 00000           PAI
41112  0604 00 0 45135           STI LIES       IND TO STOR FOR CHECK
41113  0500 00 0 45135           CLA LIES
41114  0340 00 0 45101           CAS BS135      DID WE LOAD ALL ONES...
41115  0020 00 0 41117           TRA *+2        NO- ERROR
41116  0020 00 0 41120           TRA *+2        YES- OK-GO ON.
41117  0074 00 4 00105           TSX ERROR,4
41120  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41121  0020 00 0 41105           TRA SI25       REPEAT TEST
```

ASSUMING THAT LDI CLEARED SI REG, THE PAI INST FAILED TO CONDITION THE AC TO SR COMMAND LINE.

S E C T I O N T H R E E

TESTING PAI TO CONDITION THE ELECTRONIC RESET OF SI COMMAND LINE, 2.12.64***

```
41122  472131606060              BCD 1PAI
41123  0074 00 4 45152   SI26    TSX  CLEAR,4
41124  0441 00 0 45101           LDI BS135      LOAD SI REG
41125 -0754 00 0 00000           PXD            CLEAR ACC
41126  0044 00 0 00000           PAI            CLEAR SI REG...
41127  0604 00 0 45135           STI LIES
41130 -0520 00 0 45135           NZT LIES       IS CONT LIES ZERO...
41131  0020 00 0 41134           TRA *+3        YES- OK- GO ON.
41132  0500 00 0 45135           CLA LIES       NO-
41133  0074 00 4 00105           TSX ERROR,4
41134  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41135  0020 00 0 41123           TRA SI26       REPEAT TEST
```

PAI FAILED TO CONDITION THE ELECTRONIC RESET OF SI COMMAND LINE TO COMPLETELY CLEAR ALL SI REG COLS.

TESTING OSI TO CONDITION IIS

```
41136  466231606060              BCD 1OSI
41137  0074 00 4 45152   SI27    TSX  CLEAR,4
41140  0441 00 0 45101           LDI BS135      LOAD SI REG
41141  0442 00 0 45101           OSI BS135
41142 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK.
41143  0760 00 0 00006           COM
41144  0767 00 0 00001           ALS 1          DROP Q BIT
                                  WHERE ANY OF THE SI COLS ALTERED...
41145  0100 00 0 41152           TZE *+5        NO-  OK  -GO ON.
41146  0771 00 0 00001           ARS 1          YES - ERROR
41147  0602 00 0 45135           SLW LIES
41150  0500 00 0 45135           CLA LIES
41151  0074 00 4 00105           TSX ERROR,4
41152  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41153  0020 00 0 41137           TRA SI27       REPEAT TEST
```

THE OSI INST ALTERED THE CONT OF THE SI REG WHICH HAD BEEN SET TO ALL ONES.
THE ACC S-35 INDICATE SI COLS THAT WERE ALTERED.

TESTING OSI TO CONDITION SET SI COMMAND LINES. 2.12.64

```
41154   466231606060              BCD 10SI
41155   0074 00 4 45152   SI28    TSX  CLEAR,4
41156   0560 00 0 45101           LDQ  BS135
41157   0441 00 0 45100           LDI BZERO      CLEAR SI REG 0-35
41160   0442 00 0 45101           OSI BS135
41161  -0046 00 0 00000           PIA            IND TO ACC FOR CHECK
41162   0760 00 0 00006           COM
41163   0767 00 0 00001           ALS 1          DROP Q BIT.
                                      DID WE LOAD ALL ONES TO IND...
41164   0100 00 0 41171           TZE *+5        YES -  OK  - GO ON.
41165   0771 00 0 00001           ARS 1          NO- ERROR.
41166   0602 00 0 45135           SLW LIES
41167   0500 00 0 45135           CLA LIES
41170   0074 00 4 00105           TSX ERROR,4
41171   0074 00 4 00106           TSX OK,4       CONTINUE TEST
41172   0020 00 0 41155           TRA SI28       REPEAT TEST
```

OSI FAILED TO CONDITION THE SET SI COMMAND LINES TO LOAD ALL ONES INTO SI REG.
THE ACC S-35 INDICATE SI COLS THAT WERE NOT SET.

TESTING OAI TO CONDITION IIA INST

```
41173   462131606060              BCD 10AI
41174   0074 00 4 45152   SI29    TSX  CLEAR,4
41175   0441 00 0 45101           LDI BS135      LOAD SI REG
41176  -0500 00 0 45101           CAL BS135
41177   0043 00 0 00000           OAI
41200  -0046 00 0 00000           PIA            IND TO ACC FOR CHECK.
41201   0760 00 0 00006           COM
41202   0767 00 0 00001           ALS 1          DROP Q BIT.
                                      WHERE ANY OF THE SI COLS ALTERED...
41203   0100 00 0 41211           TZE *+6        NO-  OK  - GO ON.
41204   0771 00 0 00001           ARS 1          YES-ERROR
41205   0602 00 0 45135           SLW LIES
41206   0500 00 0 45135           CLA LIES
41207   0560 00 0 45101           LDQ BS135      FOR PRINTOUT
41210   0074 00 4 00105           TSX ERROR,4
41211   0074 00 4 00106           TSX OK,4       CONTINUE TEST
41212   0020 00 0 41174           TRA SI29       REPEAT TEST
```

THE OAI INST ALTERED THE CONT OF THE SI REG WHICH HAD BEEN SET TO ALL ONES.
THE ACC S-35 INDICATES SI COLS THAT WERE ALTERED.

TESTING OAI TO CONDITION SET SI COMMAND LINES. 2.12.64

```
41213  462131606060                BCD 10AI
41214  0074 00 4 45152     SI30    TSX  CLEAR,4
41215  0441 00 0 45100             LDI BZERO      CLEAR SI REG 0-35
41216 -0500 00 0 45101             CAL BS135
41217  0043 00 0 00000             OAI            LOAD SI REG
41220 -0046 00 0 00000             PIA            IND TO ACC FOR CHECK.
41221  0602 00 0 45135             SLW LIES
                                       DID WE SET ANY SI COLS...
41222 -0100 00 0 41226             TNZ *+4        YES- OK - GO ON.
41223  0500 00 0 45135             CLA LIES       NO- ERROR.
41224  0560 00 0 45101             LDQ BS135
41225  0074 00 4 00105             TSX ERROR,4
41226  0074 00 4 00106             TSX OK,4       CONTINUE TEST
41227  0020 00 0 41214             TRA SI30       REPEAT TEST
```

TESTING OAI TO CONDITION AC TO SR COMMAND LINE,2.12.02

```
41230  462131606060                BCD 10AI
41231  0074 00 4 45152     SI31    TSX  CLEAR,4
41232  0441 00 0 45100             LDI BZERO      CLEAR SI REG 0-35
41233 -0500 00 0 45101             CAL BS135
41234  0043 00 0 00000             OAI            LOADING SI REG...
41235  0604 00 0 45135             STI LIES       IND TO STOR FOR CHECK
41236  0500 00 0 41234             CLA *-2
41237  0340 00 0 45135             CAS LIES
                                       DID WE ALTER CONT OF SR...
41240  0020 00 0 41242             TRA *+2        YES- OK - GO ON.
41241  0020 00 0 41243             TRA *+2        NO-ERROR
41242  0020 00 0 41245             TRA *+3        YES- OK - GO ON.
41243  0560 00 0 45101             LDQ BS135
41244  0074 00 4 00105             TSX ERROR,4
41245  0074 00 4 00106             TSX OK,4       CONTINUE TEST
41246  0020 00 0 41231             TRA SI31       REPEAT TEST
```

TESTING OAI TO SET SI AT I4 D1, 2.12.63

```
41247   462131606060              BCD 10AI
41250   0074 00 4 45152    SI32   TSX  CLEAR,4
41251   0441 00 0 45100           LDI BZERO
41252  -0754 00 0 00000           PXD             CLEAR  ACC
41253   0043 00 0 00000           OAI             ORING ZEROES...
41254   0604 00 0 45135           STI LIES        IND TO STOR FOR CHECK
41255  -0520 00 0 45135           NZT LIES
                                      DID WE SET ANY SI COLS...
41256   0020 00 0 41261           TRA *+3         NO-  OK  -GO ON.
41257   0500 00 0 45135           CLA LIES        YES-ERROR.
41260   0074 00 4 00105           TSX ERROR,4
41261   0074 00 4 00106           TSX OK,4        CONTINUE TEST
41262   0020 00 0 41250           TRA SI32        REPEAT TEST
```

TESTING OSI TO SET AT E10D1, 2.12.64

```
41263   466231606060              BCD 10SI
41264   0074 00 4 45152    SI33   TSX  CLEAR,4
41265   0441 00 0 45100           LDI BZERO       CLEAR SI REG 0-35
41266   0442 00 0 45100           OSI BZERO       ORING ZEROES...
41267   0604 00 0 45135           STI LIES        IND TO STOR FOR CHECK
41270  -0520 00 0 45135           NZT LIES
                                      DID WE SET ANY SI COLS...
41271   0020 00 0 41274           TRA *+3         NO-  OK  -GO ON.
41272   0500 00 0 45135           CLA LIES        YES-ERROR
41273   0074 00 4 00105           TSX ERROR,4
41274   0074 00 4 00106           TSX OK,4        CONTINUE TEST
41275   0020 00 0 41264           TRA SI33        REPEAT TEST
```

OSI SET SI OTHER THAN E10 D1.
THE ACC AND IND SHOULD INDICATE THE CONT OF SR BEFORE E7 TIME.

S E C T I O N T H R E E

TESTING -P RESET SI COMMAND LINE, 2.12.62

```
41276  636231030460              BCD 1TSI34
41277  0074 00 4 45152    SI34   TSX  CLEAR,4
41300  0441 00 0 45101           LDI BS135      LOAD SI REG
41301 -0500 00 0 45101           CAL BS135      ONES TO ACC
41302 -0042 00 0 00000           RIA
41303  0445 00 0 45101           RIS BS135      ALL ONES
41304  0604 00 0 45135           STI LIES       IND TO STOR FOR CHECK
41305  0500 00 0 45101           CLA BS135
41306  0340 00 0 45135           CAS LIES
                                     DID WE ALTER CONT OF SI REG...
41307  0020 00 0 41311           TRA *+2        YES-  OK  - GO ON.
41310  0020 00 0 41312           TRA *+2        NO-ERROR
41311  0020 00 0 41314           TRA *+3        YES-
41312  0500 00 0 45135           CLA LIES       PREP FOR PRINTOUT
41313  0074 00 4 00105           TSX ERROR,4
41314  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41315  0020 00 0 41277           TRA SI34       REPEAT TEST
```

USING TWO OF ITS EXECUTION LINES, THE -P RESET SI COMMAND LINE FAILED TO RESET ANY OF THE SI COLS.

TESTING -P RESET SI COMMAND LINE, 2.12.62
TO RESET ALL SI COLS FROM 1 TO 0.

```
41316  636231030560              BCD 1TSI35
41317  0074 00 4 45152    SI35   TSX  CLEAR,4
41320  0441 00 0 45101           LDI BS135      LOAD SI REG
41321 -0500 00 0 45101           CAL BS135
41322 -0042 00 0 00000           RIA
41323  0445 00 0 45101           RIS BS135
41324 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK.
41325  0602 00 0 45135           SLW LIES
                                     DID WE RESET ALL SI COLS...
41326  0100 00 0 41331           TZE *+3        YES-  OK  - GO ON.
41327  0500 00 0 45135           CLA LIES       NO-  ERROR.
41330  0074 00 4 00105           TSX ERROR,4
41331  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41332  0020 00 0 41317           TRA SI35       REPEAT TEST
```

USING TWO OF ITS EXECUTION LINES, THE -P RESET SI COMMAND LINE FAILED TO RESET ALL OF THE SI COLS.

TESTING RIS TO CONDITION -P RESET SI COMMAND LINE, 2.12.62

```
41333  636231030660              BCD 1TSI36
41334  0074 00 4 45152   SI36    TSX  CLEAR,4
41335  0441 00 0 45101           LDI BS135      LOAD SI REG
41336  0445 00 0 45101           RIS BS135
41337 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK
41340  0602 00 0 45135           SLW LIES
                                     DID WE RESET ALL SI COLS...
41341  0100 00 0 41344           TZE *+3        YES-  OK  - GO ON.
41342  0500 00 0 45135           CLA LIES       NO-  ERROR.
41343  0074 00 4 00105           TSX ERROR,4
41344  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41345  0020 00 0 41334           TRA SI36       REPEAT TEST
```

```
          TESTING RIS TO RESET WITH ZEROES
          TESTING RIS TO CONDITION THE LDI INST

41346  513162606060              BCD 1RIS       INST +0445
41347  0074 00 4 45152    SI37   TSX  CLEAR,4
41350  0441 00 0 45101           LDI BS135      LOAD SI REG
41351  0445 00 0 45100           RIS BZERO
41352 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK
41353  0602 00 0 45135           SLW LIES
41354  0760 00 0 00006           COM
41355  0767 00 0 00001           ALS 1          DROP Q BIT
41356  0560 00 0 45101           LDQ BS135
                                     DID WE RESET ANY SI COLS...
41357  0100 00 0 41375           TZE  SI37A+3       NO-OK- GO ON .
                                                    YES-  ERROR.
                                     WAS ERROR DUE TO TIMING PULSE---
41360  0771 00 0 00001           ARS 1
41361 -0340 00 0 41351           LAS SI37+2     LOC OF *RIS BZERO*
41362  0020 00 0 41364           TRA *+2        NO-  ERROR.
41363  0020 00 0 41372           TRA SI37A      YES-TIMING ERROR
                                                NO-  ERROR.
                                     WAS ERROR DUE TO RIS CONDITIONING
                                     THE LDI INST TO CONDITION THE ELECT
                                     RESET TO RESET ALL SI COLS...
41364 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK
                                     DID WE RESET ALL SI COLS...
41365  0100 00 0 41376           TZE SI37B      YES-  ALL SI COLS RESET.
41366  0500 00 0 45135           CLA LIES       NO-  SI COL ERROR.
41367  0074 00 4 00104           TSX  ERROR-1,4
41370  0020 00 0 41347           TRA SI37       REPEAT TEST
41371  0020 00 0 41400           TRA  SI37B+2       CONTINUE TEST
       RIS RESET SOME OF THE SI COLS USING A ZERO MASK.


41372  0500 00 0 45135    SI37A CLA LIES       TIMING PULSE ERROR...
41373  0074 00 4 00104          TSX  ERROR-1,4
41374  0020 00 0 41347          TRA SI37       REPEAT TEST
41375  0020 00 0 41400          TRA  SI37B+2       CONTINUE TEST
       RIS RESET OTHER THAN E10D1. CONT OF SR PUT IN SI REG.


41376  0500 00 0 45135    SI37B CLA LIES
41377  0074 00 4 00105          TSX ERROR,4
41400  0074 00 4 00106          TSX OK,4       CONTINUE TEST.
41401  0020 00 0 41347          TRA SI37       REPEAT TEST.
           RIS CONDITIONING LDI TO CONDITION ELECTRONIC RESET
       RIS RESET SI COLS THAT WERE MASKED WITH A ZERO.
```

TESTING ONT TO CONDITION RIS,2.12.68

```
41402   636231031060              BCD 1TSI38
41403   0074 00 4 45152    SI38   TSX  CLEAR,4
41404   0441 00 0 45101           LDI BS135      LOAD SI REG
41405   0446 00 0 45101           ONT BS135
41406   0020 00 0 41407           TRA *+1        DISREGARD COND
41407  -0046 00 0 00000           PIA            OF TRANSFER.
41410   0760 00 0 00006           COM
41411   0767 00 0 00001           ALS 1          DROP Q BIT.
                                      DID WE ALTER CONT OF SI REG...
41412   0100 00 0 41417           TZE *+5        NO-  OK  -GO ON
41413   0771 00 0 00001           ARS 1          YES-ERROR,
41414   0602 00 0 45135           SLW LIES       PREPARE ACC
41415   0500 00 0 45135           CLA LIES       FOR PRINTOUT.
41416   0074 00 4 00105           TSX ERROR,4
41417   0074 00 4 00106           TSX OK,4       CONTINUE TEST
41420   0020 00 0 41403           TRA SI38       REPEAT TEST
```

IN THE EXECUTION OF THE ONT INST, THE CONT OF THE SI REG WAS ALTERED.
THE ACC S-35 INDICATE SI COLS THAT WERE ALTERED.

TESTING RIA TO ALTER CONT OF ACC

```
41421   513121606060              BCD 1RIA       INST -0042
41422   0074 00 4 45152    SI40   TSX  CLEAR,4
41423   0441 00 0 45101           LDI BS135      LOAD SI REG
41424  -0754 00 0 00000           PXD            CLEAR  ACC
41425   0760 00 0 00006           COM            ACC Q,P,1-35 ONES.
41426  -0042 00 0 00000           RIA            CLEAR SI REG...
                                      DID WE ALTER CONT OF ACC...
41427   0760 00 0 00006           COM
41430   0100 00 0 41432           TZE *+2        NO-  OK  -GO ON
41431   0074 00 4 00105           TSX ERROR,4    YES-ERROR
41432   0074 00 4 00106           TSX OK,4       CONTINUE TEST
41433   0020 00 0 41422           TRA SI40       REPEAT TEST
```

RIA ALTERED THE CONT OF ACC. FAILURE IN PR 7 COULD CAUSE RIA TO CONDITION PIA. ACC Q,P,1-35 SHOULD CONTAIN ALL ONES.

TESTING RIA TO CONDITION-P RESET SI COMMAND LINE,2.12.62

```
41434  513121606060              BCD 1RIA       INST -0042
41435  0074 00 4 45152    SI41   TSX  CLEAR,4
41436  0441 00 0 45101           LDI BS135      LOAD SI REG
41437 -0500 00 0 45101           CAL BS135      ONES-ACC P-35.
41440 -0042 00 0 00000           RIA
41441 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK
41442 -0340 00 0 45101           LAS BS135
                                     DID WE RESET ANY SI COLS...
41443  0020 00 0 41445           TRA *+2        YES-  OK  -GO ON.
41444  0020 00 0 41446           TRA *+2        NO-ERROR
41445  0020 00 0 41451           TRA *+4        YES-  OK  -GO ON.
41446  0602 00 0 45135           SLW LIES
41447  0500 00 0 45135           CLA LIES
41450  0074 00 4 00105           TSX ERROR,4
41451  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41452  0020 00 0 41435           TRA SI41       REPEAT TEST
```

RIA FAILED TO CONDITION THE-P RESET SI COMMAND LINE TO RESET ANY OF THE SI COLS.

TESTING RIA TO CONDITION AC TO SR COMMAND LINE,2.12.02

```
41453  513121606060              BCD 1RIA       INST -0042
41454  0074 00 4 45152    SI42   TSX  CLEAR,4
41455  0441 00 0 45101           LDI BS135      LOAD SI REG
41456 -0500 00 0 45101           CAL BS135
41457 -0042 00 0 00000           RIA
41460 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK.
41461  0602 00 0 45135           SLW LIES
41462  0500 00 0 45135           CLA LIES
                                     DID WE ALTER CONT OF SR...
41463  0340 00 0 41457           CAS SI42+3     LOC OF *RIA*
41464  0020 00 0 41466           TRA *+2        YES-  OK  -GO ON.
41465  0020 00 0 41467           TRA *+2        NO-ERROR
41466  0020 00 0 41470           TRA *+2        YES-  OK  - GO ON.
41467  0074 00 4 00105           TSX ERROR,4
41470  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41471  0020 00 0 41454           TRA SI42       REPEAT TEST
```

RIA FAILED TO CONDITION AC TO SR COMMAND LINE TO ALTER CONTENTS OF SR.

```
          TESTING RIA TO CONDITION -P RESET SI COMMAND LINE,2.12.62
          TO RESET ALL SI COLS.
41472  513121606060                BCD 1RIA       INST -0042
41473  0074 00 4 45152    SI43     TSX  CLEAR,4
41474  0441 00 0 45101             LDI BS135      LOAD SI REG
41475 -0500 00 0 45101             CAL BS135
41476 -0042 00 0 00000             RIA
41477 -0046 00 0 00000             PIA            IND TO ACC FOR CHECK.
                                       DID WE RESET ALL SI COLS...
41500  0100 00 0 41504             TZE *+4        YES-  OK  -GO ON.
41501  0602 00 0 45135             SLW LIES       NO-ERROR
41502  0500 00 0 45135             CLA LIES
41503  0074 00 4 00105             TSX ERROR,4
41504  0074 00 4 00106             TSX OK,4       CONTINUE TEST
41505  0020 00 0 41473             TRA SI43       REPEAT TEST
       RIA FAILED TO CONDITION -P RESET SI COMMAND LINE TO RESET
    ALL COLS.



          TESTING RIA TO RESET SI COLS WITH A ZERO MASK---
41506  513121606060                BCD 1RIA       -0042
41507  0074 00 4 45152    SI44     TSX  CLEAR,4
41510  0441 00 0 45101             LDI BS135      LOAD SI REG
41511 -0754 00 0 00000             PXD            CLEAR  ACC
41512 -0042 00 0 00000             RIA
41513 -0046 00 0 00000             PIA            IND TO ACC FOR CHECK.
41514  0602 00 0 45135             SLW LIES       SAVE FOR PRINTOUT
41515  0760 00 0 00006             COM
41516  0767 00 0 00001             ALS 1          DROP Q BIT
                                       DID WE RESET ANY SI COLS...
41517  0100 00 0 41532             TZE SI44A+2    NO-  OK  - GO ON.
                                       WAS ERROR DUE TO TIMING PULSE...
41520  0771 00 0 00001             ARS 1
41521 -0340 00 0 41512             LAS SI44+3     CONT SR BEFORE I4D1
41522  0020 00 0 41524             TRA *+2        NO-SI COL ERROR.
41523  0020 00 0 41530             TRA SI44A      YES-ERROR, TIMING PULSE.
41524  0500 00 0 45135             CLA LIES
41525  0074 00 4 00104             TSX  ERROR-1,4
41526  0020 00 0 41507             TRA SI44       REPEAT TEST
41527  0020 00 0 41532             TRA  SI44A+2
       RIA RESET SOME OF THE SI COLS USING A ZERO MASK.

41530  0500 00 0 45135    SI44A    CLA LIES
41531  0074 00 4 00105             TSX ERROR,4
41532  0074 00 4 00106             TSX OK,4       CONTINUE TEST
41533  0020 00 0 41507             TRA SI44       REPEAT TEST
       RIA RESET OTHER THAN I4D1. CONT OF SR PUT IN SI REG.
```

TESTING INVERT SI COMMAND LINES, 2.12.62

```
41534   636231040560            BCD 1TSI45
41535   0074 00 4 45152   SI45  TSX  CLEAR,4
41536   0441 00 0 45100         LDI BZERO      CLEAR SI REG 0-35
41537   0440 00  045101         IIS BS135
41540   0604 00 0 45135         STI LIES       IND TO STOR FOR CHECK.
41541  -0500 00 0 45100         CAL  BZERO
41542   0044 00 0 00000         PAI
41543  -0500 00 0 45101         CAL BS135
41544   0041 00 0 00000         IIA
41545  -0046 00 0 00000         PIA            IND TO ACC FOR CHECK
41546  -0602 00 0 45135         ORS LIES
41547   0520 00 0 45135         ZET LIES
                                    DID WE INVERT ANY SI COLS...
41550   0020 00 0 41553         TRA *+3        YES-  OK  - GO ON.
41551   0500 00 0 45135         CLA LIES       NO-  ERROR.
41552   0074 00 4 00105         TSX ERROR,4
41553   0074 00 4 00106         TSX OK,4       CONTINUE TEST
41554   0020 00 0 41535         TRA SI45       REPEAT TEST
```

USING TWO OF ITS EXECUTION LINES, THE +P INVERT SI COMMAND LINE FAILED TO INVERT ANY OF THE SI COLS.

TESTING THE INVERT SI COMMAND LINE TO INVERT ALL SI COLS FROM ONES TO ZEROS, 2.12.62

```
41555   636231040660            BCD 1TSI46
41556   0074 00 4 45152   SI46  TSX  CLEAR,4
41557  -0500 00 0 45101         CAL  BS135
41560   0044 00 0 00000         PAI
41561   0440 00  045101         IIS BS135
41562   0604 00 0 45135         STI LIES       IND TO STOR FOR CHECK.
41563   0441 00 0 45101         LDI BS135      LOAD SI REG.
41564  -0500 00 0 45101         CAL BS135
41565   0041 00 0 00000         IIA
41566  -0046 00 0 00000         PIA            IND TO ACC FOR CHECK
41567  -0602 00 0 45135         ORS LIES
41570  -0520 00 0 45135         NZT LIES
                                    DID WE INVERT ALL SI COLS-1 TO 0...
41571   0020 00 0 41574         TRA *+3        YES-  OK  -GO ON.
41572   0500 00 0 45135         CLA LIES       NO-ERROR
41573   0074 00 4 00105         TSX ERROR,4
41574   0074 00 4 00106         TSX OK,4       CONTINUE TEST
41575   0020 00 0 41556         TRA SI46       REPEAT TEST
```

THE INVERT SI COMMAND LINE FAILED TO INVERT ALL THE SI COLS FROM ONES TO ZEROES.

THE ACC S-35 INDICATE SI COLS THAT WERE INVERTED. THE CONT OF INDICATORS INDICATE CONDITION FOR THE IIA INST ONLY.

TESTING INVERT SI COMMAND LINE TO INVERT ALL
SI COLS FROM ZEROES TO ONES, 2.12.62

```
41576   636231040760              BCD 1TSI47
41577   0074 00 4 45152   SI47    TSX  CLEAR,4
41600   0441 00 0 45100           LDI BZERO      CLEAR SI REG 0-35
41601   0560 00 0 45101           LDQ BS135      CORR CONT OF SI REG..
41602   0440 00  045101           IIS BS135
41603   0604 00 0 45135           STI LIES       IND TO STOR FOR CHECK.
41604   0441 00 0 45100           LDI BZERO      CLEAR SI REG.
41605  -0500 00 0 45101           CAL BS135
41606   0041 00 0 00000           IIA
41607  -0046 00 0 00000           PIA            IND TO ACC FOR CHECK.
41610  -0602 00 0 45135           ORS LIES
41611   0500 00 0 45135           CLA LIES
41612   0340 00 0 45101           CAS BS135
                                      DID WE INVERT ALL SI COLS...
41613   0020 00 0 41615           TRA *+2        NO- ERROR
41614   0020 00 0 41616           TRA *+2        YES-  OK  -GO ON.
41615   0074 00 4 00105           TSX ERROR,4
41616   0074 00 4 00106           TSX OK,4       CONTINUE TEST
41617   0020 00 0 41577           TRA SI47       REPEAT TEST
```

TESTING IIS TO CONDITION THE SI INVERT COMMAND LINE
TO INVERT ONES TO ZEROES.

```
41620   313162606060              BCD 1IIS       INST +0440
41621   0074 00 4 45152   SI48    TSX  CLEAR,4
41622   0441 00 0 45101           LDI BS135      LOAD SI REG
41623   0440 00  045101           IIS BS135
41624  -0046 00 0 00000           PIA            IND TO ACC FOR CHECK
41625   0602 00 0 45135           SLW LIES       SAVE FOR PRINTOUT
41626   0760 00 0 00006           COM
41627   0767 00 0 00001           ALS 1          DROP Q BIT
                                      DID WE INVERT ANY SI COLS...
41630  -0100 00 0 41633           TNZ *+3        YES-  OK  -GO ON
41631   0500 00 0 45135           CLA LIES       NO-ERROR
41632   0074 00 4 00105           TSX ERROR,4
41633   0074 00 4 00106           TSX OK,4       CONTINUE TEST
41634   0020 00 0 41621           TRA SI48       REPEAT TEST
```

```
          TESTING IIS TO CONDITION THE SI INVERT COMMAND LINE
                                        TO INVERT ALL ONES TO ZEROES***
41635  313162606060                BCD 1IIS       INST +0440
41636  0074 00 4 45152    SI49      TSX  CLEAR,4
41637  0441 00 0 45101              LDI BS135      LOAD SI REG
41640  0440 00  045101              IIS BS135
41641 -0046 00 0 00000              PIA            IND TO ACC FOR CHECK
41642  0602 00 0 45135              SLW LIES       SAVE FOR PRINTOUT
                                        DID WE INVERT ALL SI COLS...
41643  0100 00 0 41654              TZE SI49A+1    YES-  OK  - GO ON.
41644  0500 00 0 45135              CLA LIES       NO-ERROR
                                        WAS ERROR DUE TO TIMING PULSE...
41645  0340 00 0 41637              CAS SI49+1     CONT OF SR BEFORE E7.
41646  0020 00 0 41650              TRA *+2        NO-INVERT ERROR
41647  0020 00 0 41653              TRA SI49A      YES-TIMING ERROR
41650  0074 00 4 00104              TSX  ERROR-1,4
41651  0020 00 0 41636              TRA SI49       REPEAT TEST
41652  0020 00 0 41654              TRA  SI49A+1     CONTINUE TEST
       IIS FAILED TO INVERT ALL SI COLS FROM ONES TO ZEROES.

41653  0074 00 4 00105    SI49A     TSX ERROR,4
41654  0074 00 4 00106              TSX OK,4       CONTINUE TEST
41655  0020 00 0 41636              TRA SI49       REPEAT TEST
       IIS INVERTED SI COL OTHER THAN E10D1. CONT OF SI REG
    WERE INVERTED TWICE.



          TESTING IIS TO CONDITION THE SI INVERT COMMAND LINE
                                        TO INVERT ALL ZEROES TO ONES***
41656  313162606060                BCD 1IIS       INST +0440
41657  0074 00 4 45152    SI50      TSX  CLEAR,4
41660  0441 00 0 45100              LDI BZERO      CLEAR SI REG 0-35
41661  0440 00  045101              IIS BS135
41662 -0046 00 0 00000              PIA            IND TO ACC FOR CHECK
41663  0760 00 0 00006              COM
41664  0602 00 0 45135              SLW LIES       SAVE FOR PRINTOUT
41665  0560 00 0 45101              LDQ BS135      CORR CONT OF SI REG..
41666  0500 00 0 45135              CLA LIES       CONT COLS NOT INV.
                                        DID WE INVERT ALL SI COLS...
41667  0100 00 0 41671              TZE *+2        YES-  OK  - GO ON.
41670  0074 00 4 00105              TSX ERROR,4
41671  0074 00 4 00106              TSX OK,4       CONTINUE TEST
41672  0020 00 0 41657              TRA SI50       REPEAT TEST
```

```
                TESTING IIS TO INVERT SI COLS USING A ZERO MASK
41673   313162606060                    BCD 1IIS        INST +0440

41674   0074 00 4 45152     SI51        TSX  CLEAR,4
41675   0441 00 0 45100                 LDI BZERO       CLEAR SI REG 0-35
41676   0440 00  045100                 IIS BZERO
41677  -0046 00 0 00000                 PIA             IND TO ACC FOR CHECK
                                            DID WE INVERT ANY SI COLS...
41700   0100 00 0 41704                 TZE *+4         NO-  OK  -GO ON
41701   0602 00 0 45135                 SLW LIES        YES-ERROR
41702   0500 00 0 45135                 CLA LIES        COLS INVERTED S-35
41703   0074 00 4 00105                 TSX ERROR,4
41704   0074 00 4 00106                 TSX OK,4        CONTINUE TEST
41705   0020 00 0 41674                 TRA SI51        REPEAT TEST


          TESTING IIA TO CONDITION THE INVERT SI COMMAND LINE
                                  TO INVERT ONES TO ZEROES***

41706   313121606060                    BCD 1IIA        INST +0041
41707   0074 00 4 45152     SI52        TSX  CLEAR,4
41710   0441 00 0 45101                 LDI BS135
41711  -0500 00 0 45101                 CAL BS135       ONES -  ACC P-35
41712   0041 00 0 00000                 IIA
41713  -0046 00 0 00000                 PIA             IND TO ACC FOR CHECK.
41714   0602 00 0 45135                 SLW LIES        SAVE
41715   0760 00 0 00006                 COM
41716   0767 00 0 00001                 ALS 1           DROP Q BIT
                                            DID WE INVERT ANY SI COLS...
41717  -0100 00 0 41722                 TNZ *+3         YES-  OK  -GO ON
41720   0500 00 0 45135                 CLA LIES        NO-ERROR
41721   0074 00 4 00105                 TSX ERROR,4
41722   0074 00 4 00106                 TSX OK,4        CONTINUE TEST
41723   0020 00 0 41707                 TRA SI52        REPEAT TEST
```

TESTING IIA TO CONDITION THE ACC TO SR COMMAND LINE

```
41724  313121606060              BCD 1IIA       INST +0041
41725  0074 00 4 45152   SI53    TSX  CLEAR,4
41726  0441 00 0 45100           LDI BZERO      CLEAR SI REG 0-35
41727 -0500 00 0 45101           CAL BS135
41730  0041 00 0 00000           IIA
41731  0604 00 0 45135           STI LIES       IND TO STOR FOR CHECK.
41732  0500 00 0 45135           CLA LIES
41733  0340 00 0 41730           CAS *-3        CONT OF SR BEFORE GATING.
                                      DID WE ALTER CONT OF SR...
41734  0020 00 0 41736           TRA *+2        YES- OK -GO ON.
41735  0020 00 0 41737           TRA *+2        NO-ERROR
41736  0020 00 0 41740           TRA *+2        YES- OK - GO ON.
41737  0074 00 4 00105           TSX ERROR,4
41740  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41741  0020 00 0 41725           TRA SI53       REPEAT TEST
```

IIA FAILED TO CONDITION THE AC TO SR COMMAND LINE TO ALTER THE CONTENTS OF THE SR.

TESTING IIA TO INVERT SI AT I4D1

```
41742  313121606060              BCD 1IIA       INST +0041
41743  0074 00 4 45152   SI54    TSX  CLEAR,4
41744  0441 00 0 45100           LDI BZERO      CLEAR SI REG 0-35
41745 -0500 00 0 45100           CAL BZERO
41746  0041 00 0 00000           IIA
41747  0604 00 0 45135           STI LIES       IND TO STOR FOR CHECK.
41750  0500 00 0 45135           CLA LIES
41751  0340 00 0 41746           CAS *-3        CONT OF SR BEFORE GATING
                                      DID WE INVERT OTHER THAN I4...
41752  0020 00 0 41754           TRA *+2        NO- OK -GO ON.
41753  0020 00 0 41755           TRA *+2        YES-ERROR
41754  0020 00 0 41756           TRA *+2        NO- OK -GO ON.
41755  0074 00 4 00105           TSX ERROR,4
41756  0074 00 4 00106           TSX OK,4       CONTINUE TEST
41757  0020 00 0 41743           TRA SI54       REPEAT TEST
```

BEGIN TESTING RT AND LT HALF SI INSTRUCTIONS

THE FOLLOWING SHOULD BE ASSUMED FUNCTIONAL ---
1- THE INVERT, RESET, AND SET SI COMMAND LINES.
2- THE SI REG COLS.

TESTING RIL TO CONDITION THE OAI INSTRUCTION TO ALTER
THE CONT OF SI REG

```
41760  513143606060            BCD 1RIL       INST -0057
41761   0074 00 4 45152   SI55  TSX  CLEAR,4
41762   0441 00 0 45100         LDI BZERO      CLEAR SI REG
41763  -0500 00 0 45101         CAL BS135      ONES- ACC P-35
41764  -0057 00  000000         RIL            ZERO MASK
41765  -0046 00 0 00000         PIA            IND TO ACC FOR CHECK

                                    DID WE SET ALL SI REG COLS...
41766  -0340 00 0 45101         LAS BS135
41767   0020 00 0 41771         TRA *+2        NO-  OK  -GO ON
41770   0020 00 0 41772         TRA *+2        YES-ERROR
41771   0020 00 0 41775         TRA *+4        NO-  OK  -GO ON
41772   0602 00 0 45135         SLW LIES
41773   0500 00 0 45135         CLA LIES
41774   0074 00 4 00105         TSX ERROR,4
41775   0074 00 4 00106         TSX OK,4       CONTINUE TEST
41776   0020 00 0 41761         TRA SI55       REPEAT TEST
```

S E C T I O N T H R E E

TESTING RIL TO CONDITION EITHER THE INVERT OR SET SI COMMAND LINE

```
41777  513143606060              BCD 1RIL       INST -0057
42000  0074 00 4 45152    SI56   TSX  CLEAR,4
42001  0441 00 0 45100           LDI BZERO      CLEAR SI REG.
42002 -0057 00  777777           RIL 777777
42003 -0046 00 0 00000           PIA            IND TO ACC FOR CHECK
                                     DID WE ALTER CONT OF SI REG...
42004  0100 00 0 42010           TZE *+4        NO-  OK  -GO ON
42005  0602 00 0 45135           SLW LIES       YES-  ERROR
42006  0500 00 0 45135           CLA LIES
42007  0074 00 4 00105           TSX ERROR,4
42010  0074 00 4 00106           TSX OK,4       CONTINUE TEST
42011  0020 00 0 42000           TRA SI56       REPEAT TEST
```

RIL EITHER CONDITIONED THE INVERT OR SET SI COMMAND LINE.
ACC S-35 INDICATE SI COLS THAT WERE ALTERED.

TESTING SIL TO CONDITION THE PIA INST TO ALTER THE CONT OF SI REG

```
42012  623143606060              BCD 1SIL       INST -0055
42013  0074 00 4 45152    SI57   TSX  CLEAR,4
42014  0441 00 0 45101           LDI BS135      LOAD SI REG
42015 -0754 00 0 00000           PXD            CLEAR ACC
42016 -0055 00  000000           SIL            ZERO MASK
                                     DID WE ALTER CONT OF ACC...
42017  0100 00 0 42023           TZE *+4        NO-  OK  -GO ON
42020  0602 00 0 45135           SLW LIES       YES-  ERROR
42021  0500 00 0 45135           CLA LIES
42022  0074 00 4 00105           TSX ERROR,4
42023  0074 00 4 00106           TSX OK,4       CONTINUE TEST
42024  0020 00 0 42013           TRA SI57       REPEAT TEST
```

SIL CONDITIONED THE PIA INST TO ALTER CONT OF ACC.
ACC S-35 INDICATE COLS THAT WERE CHANGED FROM 1 TO 0.

TESTING SIL TO CONDITION EITHER THE INVERT OR RESET SI COMMAND LINES

```
42025  623143606060                BCD 1SIL       INST -0055
42026   0074 00 4 45152    SI58    TSX  CLEAR,4
42027   0441 00 0 45101            LDI BS135      LOAD SI REG
42030  -0055 00  777777           SIL 777777     SETTING LT HALF SI REG.
42031  -0046 00 0 00000            PIA            IND TO ACC FOR CHECK
42032   0602 00 0 45135            SLW LIES
42033   0760 00 0 00006            COM
42034   0767 00 0 00001            ALS 1          DROP Q BIT
42035   0771 00 0 00023            ARS 19         DROP 18-35
                                       DID WE ALTER CONT OF SI 0-18...
42036   0100 00 0 42042            TZE *+4        NO-  OK  - GO ON.
42037   0500 00 0 45135            CLA LIES
42040   0560 00 0 45101            LDQ BS135      YES-  ERROR
42041   0074 00 4 00105            TSX ERROR,4
42042   0074 00 4 00106            TSX OK,4       CONTINUE TEST
42043   0020 00 0 42026            TRA SI58       REPEAT TEST
```

TESTING SIL TO CONDITION THE PAI INSTRUCTION TO ALTER THE CONT OF SI REG

```
42044  623143606060                BCD 1SIL       INST -0055
42045   0074 00 4 45152    SI59    TSX  CLEAR,4
42046  -0500 00 0 45101            CAL BS135      ONES- ACC P-35
42047   0441 00 0 45100            LDI BZERO      CLEAR SI REG
42050  -0055 00  000000           SIL            ZERO MASK
42051  -0046 00 0 00000            PIA            IND TO ACC FOR CHECK
42052   0602 00 0 45135            SLW LIES       SAVE ACC
42053   0760 00 0 00006            COM
42054   0767 00 0 00001            ALS 1          DROP Q BIT
                                       DID WE SET ALL SI COLS TO ONES...
42055  -0100 00 0 42060            TNZ *+3        NO-  OK  -GO ON
42056   0500 00 0 45135            CLA LIES       YES-  ERROR
42057   0074 00 4 00105            TSX ERROR,4
42060   0074 00 4 00106            TSX OK,4
42061   0020 00 0 42045            TRA SI59
```

TESTING IIL TO CONDITION THE RIA INST TO GATE THE CONT OF ACC TO SR

```
42062  313143606060              BCD 1IIL       INST -0051
42063   0074 00 4 45152   SI60   TSX  CLEAR,4
42064   0441 00 0 45101          LDI BS135      LOAD SI REG
42065  -0500 00 0 45101          CAL BS135      ONES-  ACC P-35
42066  -0051 00  000000          IIL            ZERO MASK
42067  -0046 00 0 00000          PIA            IND TO ACC FOR CHECK
                                      DID WE INVERT OR RESET ALL SI COLS..
42070  -0100 00 0 42075          TNZ *+5        NO-  OK  - GO ON.
42071   0560 00 0 45101          LDQ BS135
42072   0602 00 0 45135          SLW LIES       YES-  ERROR
42073   0500 00 0 45135          CLA LIES
42074   0074 00 4 00105          TSX ERROR,4
42075   0074 00 4 00106          TSX OK,4       CONTINUE TEST
42076   0020 00 0 42063          TRA SI60       REPEAT TEST
```

TESTING RT AND LT HALF CIRCUITRY

```
42077  636231060160              BCD 1TSI61
42100   0074 00 4 45152   SI61   TSX  CLEAR,4
42101   0441 00 0 45100          LDI BZERO      CLEAR SI REG
42102   0055 00  777777          SIR 777777
42103  -0055 00  777777          SIL 777777
42104  -0046 00 0 00000          PIA            IND TO ACC FOR CHECK
                                      DID WE SET ANY SI COLS...
42105  -0100 00 0 42116          TNZ SI61A      YES-  OK  -GO ON
42106   0441 00 0 45101          LDI BS135      LOAD SI REG
42107   0057 00  777777          RIR 777777
42110  -0057 00  777777          RIL 777777
42111  -0046 00 0 00000          PIA            IND TO ACC FOR CHECK
42112   0760 00 0 00006          COM
42113   0767 00 0 00001          ALS 1          DROP Q BIT
                                      DID WE RESET ANY SI COLS...
42114  -0100 00 0 42116          TNZ SI61A      YES-  OK  -GO ON
42115   0074 00 4 00105          TSX ERROR,4
42116   0074 00 4 00106   SI61A  TSX OK,4       CONTINUE TEST
42117   0020 00 0 42100          TRA SI61       REPEAT TEST
```

TESTING RT HALF SI EXECUTION LINES

```
42120   636231060260                BCD 1TSI62
42121   0074 00 4 45152    SI62     TSX  CLEAR,4
42122   0441 00 0 45100             LDI BZERO      CLEAR SI REG
42123   0055 00  777777             SIR 777777
42124   0604 00 0 45135             STI LIES       IND TO STOR FOR CHECK
42125   0441 00 0 45101             LDI BS135      LOAD SI REG
42126   0057 00  777777             RIR 777777
42127  -0046 00 0 00000             PIA            IND TO ACC FOR CHECK
42130   0760 00 0 00006             COM
42131  -0602 00 0 45135             ORS LIES
42132  -0500 00 0 45135             CAL LIES
42133   0767 00 0 00022             ALS 18         ELIM SI COLS 0-17
                                        DID WE SET OR RESET ANY COLS 18-35..
42134  -0100 00 0 42137             TNZ *+3        YES-  OK  -GO ON
42135   0771 00 0 00022             ARS 18         RETURN.
42136   0074 00 4 00105             TSX ERROR,4
42137   0074 00 4 00106             TSX OK,4       CONTINUE TEST
42140   0020 00 0 42121             TRA SI62       REPEAT TEST
```

THE RT HALF SI EXECUTION LINE FAILED TO FUNCTION COMPLETELY TO ALTER CONT OF SI REGISTER.

TESTING SIR TO CONDITION THE SET SI COMMAND LINE

```
42141   623151606060                BCD 1SIR       INST +0055
42142   0074 00 4 45152    SI63     TSX  CLEAR,4
42143   0441 00 0 45100             LDI BZERO      CLEAR SI REG
42144   0055 00  777777             SIR 777777
42145  -0046 00 0 00000             PIA            IND TO ACC FOR CHECK
                                        DID WE SET ANY SI COLS...
42146   0767 00 0 00022             ALS 18         ELIM SI COLS 0-18.
42147  -0100 00 0 42152             TNZ *+3        YES-  OK  - GO ON.
42150   0771 00 0 00022             ARS 18         NO-  ERROR
42151   0074 00 4 00105             TSX ERROR,4
42152   0074 00 4 00106             TSX OK,4       CONTINUE TEST
42153   0020 00 0 42142             TRA SI63       REPEAT TEST
```

EITHER SIR FAILED TO CONDITION THE SET SI COMMAND LINE OR RT HALF SI EXECUTION LINE FAILED TO GATE SR TO ADD.

TESTING LT HALF SI EXECUTION LINES

```
42154   636231060221              BCD 1TSI62A
42155   0074 00 4 45152   SI62A TSX  CLEAR,4
42156   0441 00 0 45100         LDI BZERO     CLEAR SI REG.
42157  -0055 00  777777         SIL 777777
42160   0604 00 0 45135         STI LIES
42161   0441 00 0 45101         LDI BS135
42162  -0057 00  777777         RIL 777777
42163  -0046 00 0 00000         PIA
42164   0760 00 0 00006         COM
42165   0602 00 0 45135         SLW LIES
42166  -0500 00 0 45135         CAL LIES
42167   0771 00 0 00022         ARS 18        ELIM SI COLS 18-35.
                                  DID WE SET OR RESET ANY COLS 0-17
42170  -0100 00 0 42173         TNZ *+3
42171   0767 00 0 00022         ALS 18
42172   0074 00 4 00105         TSX ERROR,4
42173   0074 00 4 00106         TSX OK,4
42174   0020 00 0 42155         TRA SI62A
```

THE LT HALF SI EXECUTION LINE FAILED TO FUNCTION COMPLETELY TO ALTER THE CONT OF THE SI REG.

TESTING SIL TO CONDITION THE SET SI COMMAND LINE

```
42175   623143606060              BCD 1SIL
42176   0074 00 4 45152   SI63A TSX  CLEAR,4
42177   0441 00 0 45100         LDI BZERO     CLEAR SI REG
42200  -0055 00  777777         SIL 777777
42201  -0046 00 0 00000         PIA           IND TO ACC FOR CHECK
                                     DID WE SET ANY SI COLS...
42202   0771 00 0 00022         ARS 18        ELIMINATE SI COL 18-35
42203  -0100 00 0 42207         TNZ *+4       YES-  OK  -GO ON.
42204   0767 00 0 00022         ALS 18
42205   0560 00 0 45103         LDQ SILH1     FOR ERROR PRINTOUT.
42206   0074 00 4 00105         TSX ERROR,4
42207   0074 00 4 00106         TSX OK,4      CONTINUE TEST.
42210   0020 00 0 42176         TRA SI63A     REPEAT TEST.
```

EITHER SIL FAILED TO CONDITION THE SET SI COMM LINE OR LT HALF SI EXECUTION LINE FAILED TO GATE SR TO ADD.

TESTING SIR TO GATE ADD TO SR

```
42211  623151606060                BCD 1SIR       INST +0055
42212  0074 00 4 45152    SI64     TSX  CLEAR,4
42213  0441 00 0 45100             LDI BZERO      CLEAR SI REG
42214  0055 00  000000             SIR            ZERO MASK
42215  0046 00 0 00000             PIA            IND TO ACC FOR CHECK
                                        DID WE CLEAR SR S-17...
42216  0100 00 0 42222             TZE *+4        YES-  OK  -GO ON
42217  0602 00 0 45135             SLW LIES       NO-  ERROR
42220  0500 00 0 45135             CLA LIES
42221  0074 00 4 00105             TSX ERROR,4
42222  0074 00 4 00106             TSX OK,4       CONTINUE TEST
42223  0020 00 0 42212             TRA SI64       REPEAT TEST
```

THE SIR INST DID NOT GATE THE ADD TO SR TO CLEAR THE SR.

TESTING SIR TO COND THE SR 18-35 TO ADD P-17 COMM LINE IN ERROR.

```
42224  623151606060                BCD 1SIR       INST +0055
42225  0074 00 4 45152    SI65     TSX  CLEAR,4
42226  0441 00 0 45100             LDI BZERO      CLEAR SI REG.
42227  0055 00  777777             SIR 777777
42230 -0046 00 0 00000             PIA            IND TO ACC FOR CHECK.
42231  0602 00 0 45135             SLW LIES
42232  0771 00 0 00022             ARS 18         ELIM SI COLS 18-35
42233 -0340 00 0 45102             LAS SIRH1      LOC   000000777777
                                        DID WE SET ONES IN SI COLS 0-17...
42234  0020 00 0 42236             TRA *+2        NO-  OK  -GO ON
42235  0020 00 0 42237             TRA *+2        YES-  ERROR
42236  0020 00 0 42242             TRA *+4        NO-  OK  -GO ON
42237  0500 00 0 45135             CLA LIES
42240  0560 00 0 45102             LDQ SIRH1
42241  0074 00 4 00105             TSX ERROR,4
42242  0074 00 4 00106             TSX OK,4       CONTINUE TEST
42243  0020 00 0 42225             TRA SI65       REPEAT TEST
```

TESTING SIL TO GATE ADD TO SR COMM LINE

```
42244   623143606060              BCD 1SIL
42245   0074 00 4 45152   SI64A TSX  CLEAR,4
42246   0441 00 0 45100         LDI BZERO      CLEAR SI REG.
42247  -0055 00  000000         SIL            ZERO MASK.
42250  -0046 00 0 00000         PIA            IND TO ACC FOR CHECK.
                                                DID WE CLEAR SR S-17...
42251   0100 00 0 42255         TZE *+4        YES-  OK  -GO ON.
42252   0602 00 0 45135         SLW LIES       NO-  ERROR
42253   0500 00 0 45135         CLA LIES
42254   0074 00 4 00105         TSX ERROR,4
42255   0074 00 4 00106         TSX OK,4       CONTINUE TEST
42256   0020 00 0 42245         TRA SI64A      REPEAT TEST.
```

TESTING SIL TO COND THE SR18-35 TO ADD 18-35
COMMAND LINE IN ERROR

```
42257   623143606060              BCD 1SIL
42260   0074 00 4 45152   SI65A TSX  CLEAR,4
42261   0441 00 0 45100         LDI BZERO      CLEAR SI REG.
42262  -0055 00  777777         SIL 777777
42263   0604 00 0 45135         STI LIES       IND TO ACC FOR CHECK.
42264  -0500 00 0 45135         CAL LIES
42265   0767 00 0 00022         ALS 18         ELIM SI COLS P-17
42266  -0340 00 0 45103         LAS SILH1      LOC 777777000000
                                                DID WE SET ANY ONES IN COLS 0-17...
42267   0020 00 0 42271         TRA *+2        NO-  OK  -GO ON.
42270   0020 00 0 42272         TRA *+2        YES-  ERROR.
42271   0020 00 0 42275         TRA *+4        NO-  OK  -GO ON.
42272   0500 00 0 45135         CLA LIES
42273   0560 00 0 45103         LDQ SILH1
42274   0074 00 4 00105         TSX ERROR,4
42275   0074 00 4 00106         TSX OK,4       CONTINUE TEST
42276   0020 00 0 42260         TRA SI65A      REPEAT TEST
```

```
                TESTING RIR TO CONDITION THE RESET SI COMMAND LINE
42277   513151606060                    BCD 1RIR        INST +0057
42300   0074 00 4 45152     SI66        TSX  CLEAR,4
42301   0441 00 0 45102                 LDI SIRH1       ONES COL 18-35
42302   0057 00  777777                 RIR 777777
42303  -0046 00 0 00000                 PIA             IND TO ACC FOR CHECK
42304   0602 00 0 45135                 SLW LIES
42305   0760 00 0 00006                 COM
42306   0767 00 0 00023                 ALS 19          ELIM SI COLS 0-17.
                                            DID WE RESET ANY SI COLS 18-35
42307  -0100 00 0 42312                 TNZ *+3         YES-  OK  -GO ON
42310   0500 00 0 45135                 CLA LIES        NO-  ERROR
42311   0074 00 4 00105                 TSX ERROR,4
42312   0074 00 4 00106                 TSX OK,4        CONTINUE TEST
42313   0020 00 0 42300                 TRA SI66        REPEAT TEST
```

THE RIR INST EITHER FAILED TO CONDITION THE RESET SI COMMAND LINE OR FAILED TO GATE THE SR 18-35 TO ADD 18-35 COMMAND LINE.

```
                TESTING RIL TO CONDITION THE RESET SI COMM LINE

42314   513143606060                    BCD 1RIL
42315   0074 00 4 45152     SI66A       TSX  CLEAR,4
42316   0441 00 0 45103                 LDI SILH1       ONES COLS 0-17.
42317  -0057 00  777777                 RIL 777777
42320  -0046 00 0 00000                 PIA             IND TO ACC FOR CHECK
42321   0602 00 0 45135                 SLW LIES
42322   0760 00 0 00006                 COM
42323   0767 00 0 00001                 ALS 1           DROP Q
42324   0771 00 0 00023                 ARS 19          ELIM 18-35
                                            DID WE RESET ANY SI COLS 0-17...
42325  -0100 00 0 42330                 TNZ *+3         YES-  OK  -GO ON.
42326   0500 00 0 45135                 CLA LIES        NO-  ERROR.
42327   0074 00 4 00105                 TSX ERROR,4
42330   0074 00 4 00106                 TSX OK,4        CONTINUE TEST
42331   0020 00 0 42315                 TRA SI66A       REPEAT TEST
```

SECTION THREE

TESTING RIR TO CONDITION THE ADD TO SR COMMAND LINE

```
42332  513151606060              BCD 1RIR       INST +0057
42333  0074 00 4 45152    SI67   TSX  CLEAR,4
42334  0441 00 0 45101           LDI BS135      LOAD SI REG
42335  0057 00  777777           RIR 777777
42336 -0046 00 0 00000           PIA
42337  0602 00 0 45135           SLW LIES
42340  0760 00 0 00006           COM
42341  0602 00 0 45136           SLW LIES+1     DROP Q BIT
42342  0500 00 0 45136           CLA LIES+1
42343  0340 00 0 42335           CAS SI67+2     LOC  *RIR 777777*
                                     DID WE ALTER CONT OF SR...
42344  0020 00 0 42346           TRA *+2        YES-  OK  -GO ON
42345  0020 00 0 42347           TRA *+2        NO-  ERROR
42346  0020 00 0 42352           TRA *+4        YES-  OK  -GO ON
42347  0500 00 0 45135           CLA LIES
42350  0560 00 0 45103           LDQ SILH1      ONES S-17
42351  0074 00 4 00105           TSX ERROR,4
42352  0074 00 4 00106           TSX OK,4       CONTINUE TEST
42353  0020 00 0 42333           TRA SI67       REPEAT TEST
```

RIR FAILED TO CONDITION THE ADD TO SR COMM LINE TO ALTER THE CONTENTS OF THE SR--

TESTING RIR TO CONDITION SR 18-35 TO ADD P-17 COMMAND LINE IN ERROR.

```
42354  513151606060              BCD 1RIR       INST +0057
42355  0074 00 4 45152    SI68   TSX  CLEAR,4
42356  0441 00 0 45101           LDI BS135      LOAD SI REG
42357  0057 00  777777           RIR 777777
42360 -0046 00 0 00000           PIA
42361  0602 00 0 45135           SLW LIES
                                     DID WE RESET ALL SI COLS...
42362 -0100 00 0 42366           TNZ *+4        NO-  OK  -GO ON
42363  0500 00 0 45135           CLA LIES       YES-  ERROR.
42364  0560 00 0 45103           LDQ SILH1      ONES S-17
42365  0074 00 4 00105           TSX ERROR,4
42366  0074 00 4 00106           TSX OK,4       CONTINUE TEST
42367  0020 00 0 42355           TRA SI68       REPEAT TEST
```

TESTING IIR TO CONDITION THE INVERT SI COMMAND LINE

```
42370  313151606060              BCD 1IIR       INST  +0051
42371  0074 00 4 45152    SI69   TSX  CLEAR,4
42372  0441 00 0 45100           LDI BZERO      CLEAR SI REG
42373  0051 00  777777           IIR 777777
42374 -0046 00 0 00000           PIA
42375  0602 00 0 45135           SLW LIES
                                     DID WE INVERT ANY SI COLS...
42376 -0100 00 0 42402           TNZ *+4        YES-  OK  -GO ON
42377  0500 00 0 45135           CLA LIES       NO-  ERROR
42400  0560 00 0 45102           LDQ SIRH1      ONES 18-35
42401  0074 00 4 00105           TSX ERROR,4
42402  0074 00 4 00106           TSX OK,4       CONTINUE TEST
42403  0020 00 0 42371           TRA SI69       REPEAT TEST
```

TESTING TIO TO CONDITION THE TRA EXECUTION LINES
IN TRAPPING MODE.

```
42404  633146406060              BCD 1TIO-      INST +0046
42405  0074 00 4 45152   SI70    TSX  CLEAR,4
42406  0760 00 0 00007           ETM            TRAP ON TRA INST.
42407  0441 00 0 45101           LDI BS135      IDEAL
42410 -0500 00 0 45100           CAL BZERO           CONDITIONS.
42411  0774 00 2 42414           AXT SI700+1,2    ADJUSTING TRAPS FOR RET
42412  0634 00 2 45202           SXA TRAPS,2        IN CASE OF TRANSFER.
42413  0042 00 0 42414   SI700   TIO *+1        DISREGARD TRA COND.
42414 -0760 00 0 00007           LTM            --GOOD MOVE--
42415  0534 00 2 00000           LXA 0,2        ADDR OF 00000 TO XRB.
                                 IN TRAP MODE ALL TRA INSTS SHOULD
                                 STORE THEIR LOC IN ADR OF LOC 00000.
42416 -3 00000 2 42422           TXL SI70A,2,0 SHOULD NOT BE ZERO.
                                 DID WE STORE CORR TRAP ADDR....
42417  3 42413 2 42425           TXH SI70B,2,SI700    NO-ADDR HIGHER.
42420 -3 42412 2 42425           TXL SI70B,2,SI700-1  NO-ADDR LOWER.
42421  0020 00 0 42426           TRA SI70B+1    YES-  OK  -GO ON.


                                 ADDR AT 00000 WAS NOT ALTERED.
42422  0074 00 4 00104   SI70A   TSX  ERROR-1,4
42423  0020 00 0 42405           TRA SI70       REPEAT TEST
42424  0020 00 0 42426           TRA  SI70B+1       CONTINUE TEST
```

TIO FAILED TO CONDITION THE TRA EXECUTION LINES TO STORE ITS TRAP ADDR IN ADDR OF LOC 00000.

```
42425  0074 00 4 00105   SI70B   TSX ERROR,4
42426  0074 00 4 00106           TSX OK,4       CONTINUE TEST
42427  0020 00 0 42405           TRA SI70       REPEAT TEST
```

TIO CONDITIONED THE TRA EXECUTION LINES, BUT FAILED TO STORE THE CORRECT TRAP ADDRESS AT LOC 00000.

TESTING TIF TO CONDITION THE TRA EXECUTION LINES
IN TRAPPING MODE.

```
42430  633126606060              BCD 1TIF      INST  +0042
42431  0074 00 4 45152   SI71    TSX  CLEAR,4
42432  0760 00 0 00007           ETM           TRAP ON TRA INST.
42433  0441 00 0 45100           LDI BZERO     IDEAL
42434 -0500 00 0 45100           CAL BZERO          CONDITIONS.
42435  0774 00 2 42440           AXT SI710+1,2    ADJUSTING TRAPS FOR RET
42436  0634 00 2 45202           SXA TRAPS,2      IN CASE OF TRANSFER.
42437  0046 00 0 42440   SI710   TIF *+1       DISREGARD TRA COND.
42440 -0760 00 0 00007           LTM           -- GOOD MOVE.--
42441  0534 00 2 00000           LXA 0,2       ADDR OF 00000 TO XRB.
                                 IN TRAP MODE ALL TRA INSTS SHOULD
                                 STORE THERE LOC IN ADDR OF LOC 00000.
42442 -3 00000 2 42446           TXL SI71A,2,0 SHOULD NOT BE ZERO.
                                 DID WE STORE CORR TRAP ADDR...
42443  3 42437 2 42451           TXH SI71B,2,SI710    NO- ADDR HIGHER.
42444 -3 42436 2 42451           TXL SI71B,2,SI710-1  NO- ADDR LOWER.
42445  0020 00 0 42452           TRA SI71B+1   YES- OK-GO ON.


42446  0074 00 4 00104   SI71A   TSX  ERROR-1,4
42447  0020 00 0 42431           TRA SI71      REPEAT TEST.
42450  0020 00 0 42452           TRA  SI71B+1     CONTINUE TEST
```

TIF FAILED TO CONDITION THE TRA EXECUTION LINES TO STORE
ITS TRAP ADDRESS IN ADDR OF LOC 00000.

```
42451  0074 00 4 00105   SI71B   TSX ERROR,4
42452  0074 00 4 00106           TSX OK,4      CONTINUE TEST
42453  0020 00 0 42431           TRA SI71      REPEAT TEST
```

TIF CONDITIONED THE TRA EXECUTION LINES, BUT FAILED
TO STORE THE CORRECT TRAP ADDRESS AT LOC 00000.

TESTING THE 6 SKIP SI INST TO CONDITION THE TRA
EXECUTION LINES IN TRAPPING MODE.

```
42454  635147234260              BCD 1TRPCK
42455  0074 00 4 45152   SI72    TSX  CLEAR,4
42456  0774 00 2 42464           AXT SI72A+1,2 SET TRAPS FOR RETURN
42457  0634 00 2 45202           SXA TRAPS,2
42460  0774 00 1 00006           AXT 6,1        LOAD XRA FOR XEC.
42461 -0754 00 0 00000           PXD            CLEAR ACC.
42462  0760 00 0 00007           ETM            TRAP ON ERROR...

42463  0522 00 1 42503   SI72A   XEC SI72B+6,1  6 SI SKIP INST.

42464  0761 00 0 00000           NOP            DISREGARD SKIP CONDITIONS.
42465 -0760 00 0 00007           LTM            -- GOOD MOVE --
42466  0534 00 2 00000           LXA 0,2        ADDR OF LOC 00000
42467  0754 00 2 00000           PXA 0,2             TO ACC.
                                     DID WE STORE AN ADDR AT LOC 00000.
42470  0100 00 0 42473           TZE SI72E
                                                  YES-  ERROR.

42471  0074 00 4 00104           TSX ERROR-1,4
42472  0761 00 0 42455           NOP SI72

    A SI SKIP INST CAUSED FALSE TRAPPING BY STORING AN ADDR
  IN COLS 21-35 OF LOCATION 00000.
42473  2 00001 1 42461   SI72E   TIX SI72A-2,1,1 REDUCE ONE-REPEAT.
42474  0020 00 0 42504           TRA SI72D      INTERROGATE OK.

42475  0054 00  000000   SI72B   RFT            SIX
42476  0056 00  000000           RNT               SI
42477 -0054 00  000000           LFT                 SKIP
42500 -0056 00  000000           LNT                      INSTRUCTIONS.
42501  0444 00 0 45100           OFT BZERO      THESE TWO INST
42502  0446 00 0 45100           ONT BZERO        SHOULD HAVE NO EFFECT.
42503  635147255151              BCD 1TRPERR

    A SI SKIP INST CAUSED FALSE TRAPPING BY STORING AN
  ADDR IN COLS 21-35 OF LOCATION 00000. THE ADDR STORED IS NOT THE
  ADDR THAT SHOULD HAVE BEEN STORED IN THIS LOCATION.
42504  0074 00 4 00106   SI72D   TSX OK,4        CONTINUE TEST.
42505  0020 00 0 42455           TRA SI72       REPEAT TEST.
```

TESTING TIO AND TIF TO CONDITION THE CARRY TO ADDER 35 CONTROL LINE AND RELATED CIRCUITRY.

INITIAL CONDITIONS WILL BE SUCH THAT EITHER THE CONT OF ACC SI REG WILL CAUSE TRA.

```
42506  636231070460              BCD 1TSI74
42507   0074 00 4 45152   SI74   TSX  CLEAR,4
42510  -0500 00 0 45100          CAL BZERO
42511   0441 00 0 45101          LDI BS135
                                  DID COND TRA FUNCTION...
42512   0042 00 0 42517          TIO SI74A+1   YES-  OK  -GO ON.
42513  -0500 00 0 45100          CAL BZERO     NO-  TRY TIF.
42514   0441 00 0 45100          LDI BZERO
                                  DID COND TRA FUNCTION...
42515   0046 00 0 42517          TIF SI74A+1   YES-  OK  - GO ON.
42516   0074 00 4 00105   SI74A  TSX ERROR,4   NO- NEITHER INST DID.
42517   0074 00 4 00106          TSX OK,4      CONTINUE TEST
42520   0020 00 0 42507          TRA SI74      REPEAT TEST
```

TESTING TIO TO CONDITION THE CARRY TO ADDER 35 AND RELATED CIRCUITRY TO CAUSE TIO TO TRA.

```
42521  633146606060              BCD 1TIO
42522   0074 00 4 45152   SI75   TSX  CLEAR,4
42523  -0500 00 0 45100          CAL BZERO
42524   0441 00 0 45101          LDI BS135
                                                DID COND TRA FUNCTION-
42525   0042 00 0 42527          TIO SI75A+1   YES-  OK  -GO ON.
42526   0074 00 4 00105   SI75A  TSX ERROR,4   NO-  ERROR.
42527   0074 00 4 00106          TSX OK,4      CONTINUE TEST
42530   0020 00 0 42522          TRA SI75      REPEAT TEST
```

TIO FAILED TO CONDITION THE CARRY TO ADDER 35 OR RELATED CIRCUITRY TO CAUSE THE INST TO TRA.-

TESTING TIF TO CONDITION THE CARRY TO ADDER 35 AND RELATED CIRCUITRY TO CAUSE TIF TO TRA.

```
42531  633126606060              BCD 1TIF
42532   0074 00 4 45152   SI76   TSX  CLEAR,4
42533  -0500 00 0 45100          CAL BZERO
42534   0441 00 0 45100          LDI BZERO
                                  DID COND TRA FUNCTION...
42535   0046 00 0 42537          TIF SI76A+1   YES-  OK  -GO ON.
42536   0074 00 4 00105   SI76A  TSX ERROR,4   NO-  ERROR.
42537   0074 00 4 00106          TSX OK,4      CONTINUE TEST.
42540   0020 00 0 42532          TRA SI76      REPEAT TEST.
```

TESTING TIO OR TIF TO COMP ACC TO ADD AND TO
GATE ADD TO SR.

```
42541  623107076060              BCD 1SI77
42542  0074 00 4 45152   SI77    TSX  CLEAR,4
42543 -0500 00 0 45100           CAL BZERO
42544  0441 00 0 45100           LDI BZERO      ELIM SI REG FROM TEST..
                                      DID WE COMP ACC AND GATE TO SR...
42545  0042 00 0 42552           TIO SI77A+1    YES  OK  -GO ON.
42546 -0500 00 0 45100           CAL BZERO      NO-  TRY TIF.
42547  0441 00 0 45101           LDI BS135      ELIM SI REG FROM TEST..
                                      DID WE COMP ACC AND GATE TO SR...
42550  0046 00 0 42552           TIF SI77A+1    YES-  OK  -GO ON.
42551  0074 00 4 00105   SI77A   TSX ERROR,4
42552  0074 00 4 00106           TSX OK,4       CONTINUE TEST.
42553  0020 00 0 42542           TRA SI77       REPEAT TEST.
```

BOTH TIO AND TIF FAILED TO COMP ACC TO ADD OR GATE ADD TO
SR TO CAUSE TRANSFER.

TESTING TIO TO CONDITION SET SI TO SR COMM LINE

```
42554  633146606060              BCD 1TIO
42555  0074 00 4 45152   SI78    TSX  CLEAR,4
42556 -0500 00 0 45101           CAL BS135      ELIM ACC REG...
42557  0441 00 0 45101           LDI BS135
                                      DID WE GATE ALL ONES FROM SI-TO TRA...
42560  0042 00 0 42563           TIO *+3        YES-  OK  -GO ON.
42561  0560 00 0 45101           LDQ BS135      NO-  ERROR.
42562  0074 00 4 00105           TSX ERROR,4
42563  0074 00 4 00106           TSX OK,4       CONTINUE TEST.
42564  0020 00 0 42555           TRA SI78       REPEAT TEST.
```

TIO FAILED TO CONDITION THE SI REG TO SR COMM LINE TO
CAUSE TIO TO TRA.

CHECKING TIO TO ALTER CONTENTS OF ACC
ACC WILL BE ALL ZEROES.

```
42565  633146606060              BCD 1TIO
42566  0074 00 4 45152   SI79    TSX  CLEAR,4
42567 -0500 00 0 45100           CAL BZERO
42570  0441 00 0 45100           LDI BZERO
42571  0042 00 0 42572           TIO *+1
42572 -0100 00 0 42574           TNZ *+2        ACC SHOULD BE ZERO.
42573  0120 00 0 42575           TPL *+2        ACC S SHOULD BE PLUS.
42574  0074 00 4 00105           TSX ERROR,4
42575  0074 00 4 00106           TSX OK,4       CONTINUE TEST
42576  0020 00 0 42566           TRA SI79       REPEAT TEST
```

IN THE EXECUTION OF THE TIO INST, THE CONTENTS
OF THE ACCUMULATOR WERE ALTERED.
THE ACC SHOULD HAVE ALL ZEROES.
THE COLS IN ERROR ARE INDICATED BY THE BITS IN THE ACC.

CHECKING TIO TO ALTER CONTENTS OF ACC
ACC WILL BE ALL ONES.

```
42577  633146606060              BCD 1TIO
42600  0074 00 4 45152   SI80    TSX  CLEAR,4
42601 -0754 00 0 00000           PXD            CLEAR ACC
42602  0760 00 0 00006           COM            ALL ONES Q,P,1-35.
42603 -0760 00 0 00003           SSM            ACC NOW ALL ONES.
42604  0441 00 0 45100           LDI BZERO
42605  0042 00 0 42606           TIO *+1
42606  0760 00 0 00006           COM
42607 -0100 00 0 42611           TNZ *+2        ACC Q,P,1-35 -ALL ZERO..
42610 -0120 00 0 42612           TMI  *+2
42611  0074 00 4 00105           TSX ERROR,4
42612  0074 00 4 00106           TSX OK,4       CONTINUE TEST.
42613  0020 00 0 42600           TRA SI80       REPEAT TEST.
```

IN THE EXECUTION OF THE TIO INST, THE CONTENTS
OF THE ACCUMULATOR WERE ALTERED.
THE ACC SHOULD HAVE ALL ONES.
THE COLS IN ERROR ARE INDICATED BY THE BITS IN THE ACC.

CHECKING TIF TO ALTER THE CONTENTS OF THE ACC
ACC WILL BE ALL ZEROES.

```
42614  633126606060              BCD 1TIF
42615  0074 00 4 45152   SI81    TSX  CLEAR,4
42616 -0500 00 0 45100           CAL BZERO
42617  0560 00 0 45100           LDQ BZERO
42620  0046 00 0 42621           TIF *+1
42621 -0100 00 0 42623           TNZ *+2        SHOULD BE ALL ZEROES.
42622  0120 00 0 42624           TPL *+2        SHOULD BE PLUS.
42623  0074 00 4 00105           TSX ERROR,4
42624  0074 00 4 00106           TSX OK,4       CONTINUE TEST.
42625  0020 00 0 42615           TRA SI81       REPEAT TEST.
```

IN THE EXECUTION OF THE TIF INSTRUCTION. THE CONTENTS OF THE ACCUMULATOR WERE ALTERED.
THE ACC SHOULD HAVE ALL ZEROES.
THE COLS IN ERROR ARE INDICATED BY BITS IN THE ACC.

CHECKING TIF TO ALTER THE CONTENTS OF THE ACC
ACC WILL BE ALL ONES.

```
42626  633126606060              BCD 1TIF
42627  0074 00 4 45152   SI82    TSX  CLEAR,4
42630 -0754 00 0 00000           PXD            CLEAR ACC
42631  0760 00 0 00006           COM            ONES- Q,P,1-35
42632 -0760 00 0 00003           SSM            SIGN ALSO A ONE.
42633  0441 00 0 45100           LDI BZERO
42634  0046 00 0 42635           TIF *+1
42635  0760 00 0 00006           COM
42636 -0100 00 0 42640           TNZ *+2        ACC Q,P,1-35 -ALL ZERO..
42637 -0120 00 0 42641           TMI  *+2
42640  0074 00 4 00105           TSX ERROR,4
42641  0074 00 4 00106           TSX OK,4       CONTINUE TEST
42642  0020 00 0 42627           TRA SI82       REPEAT TEST
```

IN THE EXECUTION OF THE TIF INSTRUCTION. THE CONTENTS OF THE ACCUMULATOR WERE ALTERED.
THE ACC SHOULD HAVE ALL ONES.
THE COLS IN ERROR ARE INDICATED BY BITS IN THE ACC.

S E C T I O N T H R E E

TEST TIF AND TIO

```
42643   633146633126            BCD 1TIOTIF
42644   0074 00 4 45152   SI83  TSX  CLEAR,4
42645  -0500 00 0 45114         CAL  BIT35
42646   0602 00 0 45135         SLW  LIES

42647  -0500 00 0 45135         CAL  LIES
42650   0760 00 0 00006         COM
42651   0044 00 0 00000         PAI
42652  -0500 00 0 45135         CAL  LIES
42653   0042 00 0 42665         TIO  SI83A      SHOULD NOT XFER
42654   0046 00 0 42656         TIF  *+2        SHOULD XFER
42655   0020 00 0 42665         TRA  SI83A
42656   0441 00 0 45135         LDI  LIES
42657   0046 00 0 42665         TIF  SI83A      SHOULD NOT XFER
42660   0042 00 0 42662         TIO  *+2        SHOULD XFER
42661   0020 00 0 42665         TRA  SI83A
42662   0140 00 0 42666         TOV  SI83A+1
42663   0767 00 0 00001         ALS  1
42664   0020 00 0 42646         TRA  SI83+2
42665   0074 00 4 00105   SI83A TSX  ERROR,4
42666   0074 00 4 00106         TSX  OK,4
42667   0020 00 0 42644         TRA  SI83
```

CHECKING TIO TO NOT COND TRA IN TRAPPING MODE

```
42670  633146406060              BCD 1TIO-
42671  0074 00 4 45152   SI87    TSX  CLEAR,4
42672  0760 00 0 00007           ETM
42673  0774 00 2 42703           AXT SI87A,2    TO RETURN TO TEST
42674  0634 00 2 45202           SXA TRAPS,2      ROUTINE IN CASE OF TRAP.
42675 -0500 00 0 45101           CAL BS135      CONDITIONS ARE SUCH THAT
42676  0441 00 0 45100           LDI BZERO        TIO SHOULDNT TRA.
                                     DO WE TRA IN TRAP MODE...
42677  0042 00 0 42702           TIO *+3
42700 -0760 00 0 00007           LTM              NO-  OK  -GO ON.
42701  0020 00 0 42704           TRA SI87A+1
42702 -0760 00 0 00007           LTM              IN CASE OF TRA- NO TRAP.
42703  0074 00 4 00105   SI87A   TSX ERROR,4
42704  0074 00 4 00106           TSX OK,4       CONTINUE TEST.
42705  0020 00 0 42671           TRA SI87       REPEAT TEST.
```

UNDER TEST CONDITIONS, TIO SHOULDNT HAVE TRA IN TRAP MODE.

CHECKING TIO TO TRA IN TRAPPING MODE

```
42706  633146406060              BCD 1TIO-
42707  0074 00 4 45152   SI88    TSX  CLEAR,4
42710  0760 00 0 00007           ETM
42711  0774 00 2 42720           AXT SI88A+1,2 TO RETURN AFTER A
42712  0634 00 2 45202           SXA TRAPS,2      SUCCESSFUL TRAP.
42713  0500 00 0 45100           CLA BZERO      CONDITIONS ARE SUCH THAT
42714  0441 00 0 45101           LDI BS135        TIO SHOULD TRANSFER.
                                     DID WE TRA IN TRAP MODE...
42715  0042 00 0 42716           TIO *+1        IN CASE OF TRA-DIDNT TRAP.
42716 -0760 00 0 00007           LTM              NO-  ERROR.
42717  0074 00 4 00105   SI88A   TSX ERROR,4
42720  0074 00 4 00106           TSX OK,4
42721  0020 00 0 42707           TRA SI88
```

UNDER TEST COND. TIO SHOULD HAVE TRAPPED TO LOCATION 00001.

CHECKING TIF TO NOT TRA IN TRAP MODE

```
42722  633126406060              BCD 1TIF-
42723  0074 00 4 45152    SI89   TSX  CLEAR,4
42724  0760 00 0 00007           ETM
42725  0774 00 2 42735           AXT SI89A,2    IN CASE TIF TRAPS
42726  0634 00 2 45202           SXA TRAPS,2       IN ERROR.
42727 -0500 00 0 45101           CAL BS135      CONDITIONS ARE SUCH THAT
42730  0441 00 0 45101           LDI BS135      TIF SHOULDNT TRA.
                                     DO WE TRA IN TRAP MODE...
42731  0046 00 0 42734           TIF *+3
42732 -0760 00 0 00007           LTM               NO-  OK  -GO ON.
42733  0020 00 0 42736           TRA SI89A+1
42734 -0760 00 0 00007           LTM               IN CASE TRA-DIDNT TRAP.
42735  0074 00 4 00105    SI89A  TSX ERROR,4
42736  0074 00 4 00106           TSX OK,4       CONTINUE TEST.
42737  0020 00 0 42723           TRA SI89       REPEAT TEST.
```

UNDER TEST COND, TIF SHOULDNT TRA IN TRAP MODE.

CHECKING TIF TO TRA IN TRAPPING MODE

```
42740  633126406060              BCD 1TIF-
42741  0074 00 4 45152    SI90   TSX  CLEAR,4
42742  0760 00 0 00007           ETM
42743  0774 00 2 42752           AXT SI90A+1,2 TO RETURN AFTER A
42744  0634 00 2 45202           SXA TRAPS,2      SUCCESSFUL TRAP.
42745  0500 00 0 45100           CLA BZERO      CONDITIONS ARE SUCH THAT
42746  0441 00 0 45100           LDI BZERO         TIF SHOULD TRA.
                                     DO WE TRA IN TRAP MODE...
42747  0046 00 0 42750           TIF *+1        IN CASE OF TRA- DIDNT TRAP.
42750 -0760 00 0 00007           LTM               NO-  ERROR---
42751  0074 00 4 00105    SI90A  TSX ERROR,4
42752  0074 00 4 00106           TSX OK,4
42753  0020 00 0 42741           TRA SI90
```

UNDER TEST COND, TIF SHOULD HAVE TRAP TO LOCATION 00001.

TEST THAT NEITHER TIF NOR TIO MODIFIES CONTENTS OF INDICATOR REGISTER

```
42754  633126633146              BCD 1TIFTIO
42755  0754 00 0 00000    IOF    PXA  ,,          CLEAR ACC
42756  0760 00 0 00006           COM
42757  0131 00 0 00000           XCA               ALL BITS BUT SIGN
42760 -0600 00 0 45135           STQ  TEMP         ALL BITS BUT ONE

42761  0441 00 0 45135           LDI  TEMP         TEST WORD TO INDS
42762  0754 00 0 00000           PXA  ,,           CLEAR ACC
42763  0046 00 0 42765           TIF  *+2          SHOULD TRANSFER
42764  0020 00 0 42766           TRA  *+2
42765  0042 00 0 42770           TIO  *+3          SHOULD TRANSFER
42766  0074 00 4 00104           TSX  ERROR-1,4
42767  0761 00 0 42755           NOP  IOF

42770  0760 00 0 00006           COM               ONES TO ACC  Q,P,1-35
42771  0046 00 0 42774           TIF  *+3          SHOULD NOT TRANSFER
42772  0042 00 0 42774           TIO  *+2          SHOULD NOT TRANSFER
42773  0020 00 0 42776           TRA  *+3
42774  0074 00 4 00104           TSX  ERROR-1,4
42775  0761 00 0 42755           NOP  IOF
42776 -0046 00 0 00000           PIA               INDICATORS TO ACC

42777 -0340 00 0 45135           LAS  TEMP         SHOULD COMPARE EQUAL
43000  0020 00 0 43002           TRA  *+2
43001  0020 00 0 43004           TRA  *+3          OK
43002  0074 00 4 00104           TSX  ERROR-1,4    CONTENTS OF INDICATOR
43003  0761 00 0 42755           NOP  IOF          REGISTER WERE CHANGED

43004  0760 00 0 00161           SWT  1            TEST FOR TIGHT LOOP
43005  0020 00 0 43007           TRA  *+2          GO ON
43006  0020 00 0 42761           TRA  IOF+4
43007 -0773 00 0 00001           RQL  1
43010  0162 00 0 43012           TQP  *+2
43011  0020 00 0 42760           TRA  IOF+3
43012  0074 00 4 00106           TSX  OK,4
43013  0020 00 0 42755           TRA  IOF
```

SECTION THREE

TESTING ONT OR OFT TO CONDITION THE ADV PC COMM LINE
CONTROL WORD-ALL ONES.

```
43014  636231110160              BCD 1TSI91
43015  0074 00 4 45152   SI91    TSX  CLEAR,4
                                          DID WE ADV PC. TO SKIP...
43016  0020 00 0 43020           TRA *+2      NO-  OK  -GO ON.
43017  0074 00 4 00105   SI91A   TSX ERROR,4  YES-  ERROR
43020  0074 00 4 00106           TSX OK,4     CONTINUE TEST.
43021  0020 00 0 43015           TRA SI91     REPEAT TEST.
```

ONT OR OFT CAUSED THE MACH TO SKIP IN ERROR.

TESTING THE SIX SKIP INST TO CYCLE THE CONT OF ACC

CONTENTS OF ACC SET TO ALL ONES.

```
43022  636231110260              BCD 1TSI92
43023  0074 00 4 45152   SI92    TSX  CLEAR,4
43024 -0754 00 0 00000           PXD              CLEAR ACC
43025  0760 00 0 00006           COM              1S - Q,P,1-35.
43026 -0760 00 0 00003           SSM              ONE TO SIGN POSITION.
43027  0056 00  000000          RNT              ZERO MASK
43030  0761 00 0 00000           NOP              JUST IN CASE OF FALSE SKIP.
43031  0760 00 0 00006           COM              RESETTING TO ORIGINAL
43032  0760 00 0 00002           CHS                    CONDITIONS...
43033 -0100 00 0 43035           TNZ *+2          IF TRA-ERR IN CYCLING ACC
43034  0120 00 0 43036           TPL *+2          IF TRA-SIGN POSITION OK.
43035  0074 00 4 00105           TSX ERROR,4
43036  0074 00 4 00106           TSX OK,4         CONTINUE TEST
43037  0020 00 0 43023           TRA SI92         REPEAT TEST
```

THE CONTENTS OF ACC WAS ALTERED IN THE EXECUTION OF A SKIP INSTRUCTION. THE ACC IS CYCLED IN THE 1ST L TIME AS FOLLOWS -

ACC	Q,P-35	TO	SR	S,Q,1-35	L2 D1
SR	S,1-35	TO	ADD	P-35	L9D3
ADD	Q-35	TO	ACC	Q-35	L10 D1
SR	Q	TO	ACC	Q	L10 D1

TESTING THE SKIP INST TO COND THE CARRY TO ADDER 35
AND RELATED CIRCUITRY TO ADV PROG CTR

THE CONT OF CNTL WORD OR SI REG WILL BE SUCH THAT
EITHER WILL GATE ALL ONES WHEN 1 IS GATED TO ADDER 35

```
43040   636231110360              BCD 1TSI93
43041   0074 00 4 45152    SI93   TSX  CLEAR,4
43042   0441 00 0 45101           LDI BS135
43043   0056 00   000000          RNT              DO WE ADV P. C...
43044   0020 00 0 43046           TRA *+2            NO-  TRY RFT
43045   0020 00 0 43073           TRA SI93A          YES-  OK  -GO ON.
43046   0441 00 0 45100           LDI BZERO
43047   0054 00   000000          RFT              DO WE ADV P. C...
43050   0020 00 0 43052           TRA *+2            NO-  TRY LNT.
43051   0020 00 0 43073           TRA SI93A          YES-  OK  -GO ON.
43052   0441 00 0 45101           LDI BS135
43053  -0056 00   000000          LNT              DO WE ADV P. C...
43054   0020 00 0 43056           TRA *+2            NO-  TRY LFT
43055   0020 00 0 43073           TRA SI93A          YES-  OK  -GO ON.
43056   0441 00 0 45100           LDI BZERO
43057  -0054 00   000000          LFT              DO WE ADV P.C....
43060   0020 00 0 43062           TRA *+2          NO-  TRY ONT.
43061   0020 00 0 43073           TRA SI93A        YES-  OK  -GO ON.
43062   0441 00 0 45101           LDI BS135
43063   0446 00 0 45100           ONT BZERO        DO WE ADV P.C....
43064   0020 00 0 43066           TRA *+2          NO-  TRY OFT
43065   0020 00 0 43073           TRA SI93A        YES-  OK  -GO ON.
43066   0441 00 0 45100           LDI BZERO
43067   0444 00 0 45100           OFT BZERO        DO WE ADV P.C....
43070   0020 00 0 43072           TRA *+2          NO - COMPLETE WASHOUT.
43071   0020 00 0 43073           TRA SI93A        YES-  OK  -GO ON.
43072   0074 00 4 00105           TSX ERROR,4
43073   0074 00 4 00106    SI93A  TSX OK,4         CONTINUE TEST
43074   0020 00 0 43041           TRA SI93         REPEAT TEST
```

THE SIX SI SKIP INST FAILED TO CONDITION THE CARRY
TO ADDER 35 OR RELATED CIRCUITRY TO ADV P.C.

S E C T I O N T H R E E

TESTING ONT TO CONDITION SR 18-35 TO ADD 18-35
COMM LINE IN ERROR

```
43075   464563606060              BCD 1ONT
43076   0074 00 4 45152   SI94    TSX  CLEAR,4
43077   0441 00 0 45113           LDI BIT17      BIT IN COL 17.
43100   0446 00 0 45102           ONT SIRH1      ONES 18-35
                                                 DO WE SKIP...
43101   0020 00 0 43103           TRA *+2        NO-  OK  -GO ON.
43102   0074 00 4 00105           TSX ERROR,4    YES-ERROR
43103   0074 00 4 00106           TSX OK,4       CONTINUE TEST
43104   0020 00 0 43076           TRA SI94       REPEAT TEST
```

ONT SKIPPED IN ERROR. CONDITIONING OF THE SR 18-35 TO ADD 18-35 COMM LINE WOULD CAUSE THE ONT INST TO SKIP.

TESTING ONT TO CONDITION SR 18-35 TO ADD P-17
COMM LINE IN ERROR

```
43105   464563606060              BCD 1ONT
43106   0074 00 4 45152   SI94A   TSX  CLEAR,4
43107   0441 00 0 45114           LDI BIT35      BIT IN COL 35.
43110   0446 00 0 45106           ONT P1835      ONES - P-18 AND 35.
                                                 DO WE SKIP...
43111   0020 00 0 43113           TRA *+2        NO-  OK  -GO ON.
43112   0074 00 4 00105           TSX ERROR,4    YES-  ERROR.
43113   0074 00 4 00106           TSX OK,4       CONTINUE TEST
43114   0020 00 0 43106           TRA SI94A      REPEAT TEST
```

ONT SKIPPED IN ERROR. CONDITIONING OF THE SR 18-35 TO ADD P-17 LINE IN ERROR WOULD CAUSE THE ONT INST TO SKIP.

TESTING ONT FOR FALSE I TIME COMP OF SI REG

```
43115  464563606060              BCD 1ONT
43116  0074 00 4 45152   SI94B   TSX  CLEAR,4
43117  0441 00 0 45102           LDI SIRH1      ONES - 18-35.
43120  0446 00 0 45103           ONT SILH1      ONES - P-17.
                                                DO WE SKIP...
43121  0020 00 0 43123           TRA *+2        NO-  OK  -GO ON.
43122  0074 00 4 00105           TSX ERROR,4    YES-  ERROR.
43123  0074 00 4 00106           TSX OK,4       CONTINUE TEST.
43124  0020 00 0 43116           TRA SI94B      REPEAT TEST.
```

ONT SKIPPED IN ERROR. CONDITIONING THE OFF TEST COMP OF SI REG IN ERROR WOULD CAUSE ONT TO SKIP-

TESTING OFT TO COMPLIMENT THE SI IN I TIME

```
43125  462663606060              BCD 1OFT
43126  0074 00 4 45152   SI94C   TSX  CLEAR,4
43127  0441 00 0 45105           LDI P07S       BIT PATT - 000 111
43130  0444 00 0 45101           OFT BS135      ALL ONES.
                                                DO WE SKIP...
43131  0020 00 0 43133           TRA *+2        NO-  OK  -GO ON.
43132  0074 00 4 00105           TSX ERROR,4    YES-  ERROR.
43133  0074 00 4 00106           TSX OK,4       CONTINUE TEST
43134  0020 00 0 43126           TRA SI94C      REPEAT TEST
```

OFT SKIPPED IN ERROR. FAILURE TO COMP THE SI IN I TIME WOULD CAUSE OFT TO SKIP-

TESTING ONT,RNT,LNT TO COND THE TRUE SI REG TO SR COMM LINE

```
43135  636231110660            BCD 1TSI96
43136   0074 00 4 45152   SI96  TSX  CLEAR,4
43137  -0500 00 0 45110         CAL P52S       BIT PATT - 101 010
43140   0441 00 0 45101         LDI BS135      ALL ONES
43141   0446 00 0 45104         ONT P05S       BIT PATT - 000 101
                                               DO WE SKIP...
43142   0020 00 0 43144         TRA *+2        NO-  TRY RNT.
43143   0020 00 0 43153         TRA SI96A      YES-  OK  -GO ON.
43144   0056 00  777777         RNT 777777
                                               DO WE SKIP...
43145   0020 00 0 43147         TRA *+2        NO-  TRY LNT
43146   0020 00 0 43153         TRA SI96A      YES-  OK  -GO ON.
43147  -0056 00  777777         LNT 777777
                                               DO WE SKIP...
43150   0020 00 0 43152         TRA *+2        NO-  ALL IN ERROR.
43151   0020 00 0 43153         TRA SI96A      YES-  OK  - GO ON.
43152   0074 00 4 00105         TSX ERROR,4
43153   0074 00 4 00106   SI96A TSX OK,4        CONTINUE TEST.
43154   0020 00 0 43136         TRA SI96       REPEAT TEST.
```

ONT, RNT, LNT FAILED TO GATE TRUE SI TO SR TO ALLOW INST TO SKIP-

TESTING OFT, RFT, LFT TO COMPLIMENT SI REG IN I TIME AND
TEST THE SI REG I TIME NEXT RECOMP BY OFF TEST INSTRS

```
43155  636231110760            BCD 1TSI97
43156   0074 00 4 45152   SI97  TSX  CLEAR,4
43157  -0500 00 0 45110         CAL P52S       BIT PATT - 101 010
43160   0441 00 0 45100         LDI BZERO      ALL ZEROES
43161   0444 00 0 45104         OFT P05S       BIT PATT - 000 101
43162   0020 00 0 43164         TRA *+2        NO-  TRY RFT
43163   0020 00 0 43174         TRA SI97A      YES-  OK  -GO ON.
43164   0441 00 0 45100         LDI  BZERO
43165   0054 00  050505         RFT 050505     BIT PATT - 000 101
43166   0020 00 0 43170         TRA *+2        NO-  TRY LFT.
43167   0020 00 0 43174         TRA SI97A      YES-  OK  -GO ON.
43170   0441 00 0 45100         LDI  BZERO
43171  -0054 00  050505         LFT 050505
43172   0020 00 0 43174         TRA *+2        NO - COMPL WASHOUT.
43173   0020 00 0 43174         TRA SI97A      YES-  OK  -GO ON.
43174  -0046 00 0 00000   SI97A PIA
43175   0100 00 0 43177         TZE  *+2
43176   0074 00 4 00105         TSX ERROR,4
43177   0074 00 4 00106         TSX  OK,4      CONTINUE TEST
43200   0020 00 0 43156         TRA SI97       REPEAT TEST.
```

TESTING THE SIX SI SKIP INST TO CONDITION THE
RELATED COMM LINES TO GATE THE CONTROL WORD

CNTL WORD SHOULD CAUSE THE INST TO SKIP.

```
43201   636231111060              BCD 1TSI98
43202   0074 00 4 45152   SI98    TSX  CLEAR,4
43203  -0500 00 0 45110           CAL P52S        BIT PATT  101 010
43204   0441 00 0 45100           LDI BZERO
43205   0446 00 0 45100           ONT BZERO       DO WE SKIP...
43206   0020 00 0 43210           TRA *+2         NO-  TRY RNT
43207   0020 00 0 43235           TRA SI98A       YES-  OK  -GO ON.
43210  -0500 00 0 45110           CAL P52S
43211   0441 00 0 45100           LDI BZERO
43212   0056 00  000000           RNT             DO WE SKIP...
43213   0020 00 0 43215           TRA *+2         NO-  TRY LFT.
43214   0020 00 0 43235           TRA SI98A       YES-  OK  -GO ON.
43215  -0500 00 0 45110           CAL P52S
43216   0441 00 0 45101           LDI BS135
43217  -0054 00  000000           LFT             DO WE SKIP...
43220   0020 00 0 43222           TRA *+2         NO-  TRY LNT
43221   0020 00 0 43235           TRA SI98A       YES-  OK-  GO ON.
43222  -0500 00 0 45110           CAL P52S
43223   0441 00 0 45100           LDI BZERO
43224  -0056 00  000000           LNT             DO WE SKIP...
43225   0020 00 0 43227           TRA *+2         NO-  TRY RFT
43226   0020 00 0 43235           TRA SI98A       YES-  OK  -GO ON.
43227  -0500 00 0 45110           CAL P52S
43230   0441 00 0 45101           LDI BS135
43231   0054 00  000000           RFT             DO WE SKIP...
43232   0020 00 0 43234           TRA *+2         NO- ALL IN ERROR.
43233   0020 00 0 43235           TRA SI98A       YES-  OK  -GO ON.
43234   0074 00 4 00105           TSX ERROR,4
43235   0074 00 4 00106   SI98A   TSX OK,4        CONTINUE TEST
43236   0020 00 0 43202           TRA SI98        REPEAT TEST
```

NONE OF THE SI SKIP INST TESTED CONDITIONED THE RELATED COMM LINES TO COMPLETELY CYCLE THE CONTROL WORD CORRECTLY.

THE CNTL WORD IS CYCLED AS FOLLOWS-ALL CYCLING DONE IN 1ST L TIME - FIVE SI SKIP INST ARE USED TO FURTHER ELIM SR TO ADD-LOD3- ERROR.

```
          ADD Q-35  TO  ACC Q-35     L2  D1
     COMP ACC Q-35  TO  ADD Q-35     L4  D3
          ADD Q-35  TO  ACC Q-35     L6  D1
          ACC Q-35  TO   SR Q-35     L10 D1
```

TESTING RFT, RNT TO COND SR 18-35 TO ADD 18-35 COMM LINE

```
43237  636231111160              BCD 1TSI99
43240  0074 00 4 45152   SI99    TSX  CLEAR,4
43241  0441 00 0 45102           LDI SIRH1      ONES- 18-35
43242  0056 00  777777           RNT 777777     DO WE SKIP...
43243  0020 00 0 43245           TRA *+2        NO-  TRY RFT
43244  0020 00 0 43252           TRA SI99A      YES-  OK  -GO ON.
43245  0441 00 0 45100           LDI BZERO
43246  0054 00  777777           RFT 777777     DO WE SKIP...
43247  0020 00 0 43251           TRA *+2        NO-  ERROR.
43250  0020 00 0 43252           TRA SI99A      YES-  OK  -GO ON.
43251  0074 00 4 00105           TSX ERROR,4
43252  0074 00 4 00106   SI99A   TSX OK,4       CONTINUE TEST
43253  0020 00 0 43240           TRA SI99       REPEAT TEST
```

RNT, RFT FAILED TO CONDITION THE SR 18-35 TO ADD 18-35 COMM LINE TO CAUSE THESE INST TO SKIP.

TESTING LFT, LNT TO COND SR 18-35 TO ADD P-17 COMM LINE

```
43254  636231010000              BCD 1TSI100
43255  0074 00 4 45152   SI100   TSX  CLEAR,4
43256  0441 00 0 45103           LDI SILH1      ONES- P-17
43257 -0056 00  777777           LNT 777777     DO WE SKIP...
43260  0020 00 0 43262           TRA *+2        NO -  TRY LNT.
43261  0020 00 0 43267           TRA SI101      YES-  OK  -GO ON.
43262  0441 00 0 45100           LDI BZERO
43263 -0054 00  777777           LFT 777777     DO WE SKIP...
43264  0020 00 0 43266           TRA *+2        NO -  ERROR.
43265  0020 00 0 43267           TRA SI101      YES-  OK  -GO ON.
43266  0074 00 4 00105           TSX ERROR,4
43267  0074 00 4 00106   SI101   TSX OK,4       CONTINUE TEST.
43270  0020 00 0 43255           TRA SI100      REPEAT TEST.
```

LFT, LNT FAILED TO CONDITION THE SR 18-35 TO ADD P-17 COMM LINE TO CAUSE THESE INST TO SKIP...

TESTING SIX SI SKIP INSTR TO OPERATE PROPERLY
IN TRANSFER TRAP MODE.

```
43271   636231010002                BCD 1TSI102
43272   0074 00 4 45152    SI102    TSX  CLEAR,4
43273   0774 00 1 00014             AXT  12,1
43274   0760 00 0 00007             ETM
43275   0522 00 1 43323             XEC  SI103+12,1
43276   0522 00 1 43324             XEC  SI103+13,1
43277   0021 00 0 43302             TTR  *+3        ERROR SHOULD SKIP
43300  -0760 00 0 00007             LTM              OK
43301   0020 00 0 43305             TRA  *+4
43302  -0760 00 0 00007             LTM
43303   0074 00 4 00104             TSX  ERROR-1,4
43304   0020 00 0 43272             TRA  SI102
43305   2 00002 1 43274             TIX  SI102+2,1,2
43306   0020 00 0 43323             TRA  SI104

43307   0441 00 0 45101    SI103    LDI  BS135     SIX SI
43310   0054 00  000000             RFT
43311   0441 00 0 45101             LDI  BS135     SKIP
43312  -0054 00  000000             LFT
43313  -0500 00 0 45101             CAL  BS135        INSTRUCTIONS
43314   0444 00 0 45100             OFT  BZERO
43315   0441 00 0 45100             LDI  BZERO     USED
43316   0056 00  000000             RNT
43317   0441 00 0 45100             LDI  BZERO     IN
43320  -0056 00  000000             LNT
43321  -0500 00 0 45100             CAL  BZERO        TEST
43322   0446 00 0 45100             ONT  BZERO

43323   0074 00 4 00106    SI104    TSX  OK,4
43324   0020 00 0 43272             TRA  SI102
```

S E C T I O N T H R E E

SI INSTRUCTION RELIABILITY SECTION

RIPPLE TESTS

```
                RIPPLE TEST-CHECKING PAI AND LDI
                                        EACH COL CHECKED INDIVIDUALLY.
                WITH XRA     CHECKING
                     2          PAI
                     1          LDI

43325  472131432431                  BCD 1PAILDI
43326  0074 00 4 45152    RSI1       TSX  CLEAR,4
43327  0774 00 1 00002               AXT 2,1          FOR XEC
43330  0774 00 2 00044               AXT 36,2         STEP COUNT
43331 -0500 00 0 45114               CAL BIT35
43332  0602 00 0 45135               SLW LIES
43333 -0500 00 0 45135               CAL LIES

43334  0522 00 1 43357               XEC RSI1A+2,1 XEC PAI OR LDI.

43335  0604 00 0 45136               STI LIES+1
43336  0500 00 0 45136               CLA LIES+1
43337  0340 00 0 45135               CAS LIES
43340  0020 00 0 43342               TRA *+2          ERROR
43341  0020 00 0 43350               TRA RSI1B        OK-  TRY AGAIN.

43342  0760 00 0 00161               SWT 1            WANT A CLOSED LOOP...
43343  0020 00 0 43345               TRA *+2          UP-  NO  -GO ON.
43344  0020 00 0 43333               TRA RSI1+5       DN- YES  -REPEAT SAME VAL.

43345  0560 00 0 45135               LDQ LIES
43346  0074 00 4 00104               TSX ERROR-1,4
43347  0020 00 0 43326               TRA RSI1


43350 -0500 00 0 45135    RSI1B      CAL LIES         STEPPING BIT
43351  0767 00 0 00001               ALS 1              ONE COLUMN.
43352  2 00001 2 43332               TIX RSI1+4,2,1 KEEPING COUNT.

43353  2 00001 1 43330               TIX RSI1+2,1,1 REPEAT FOR LDI.
43354  0020 00 0 43357               TRA *+3          JUMP OVER XEC LOC.

                                                                      XRA
43355  0044 00 0 00000    RSI1A      PAI              TWO INST          2
43356  0441 00 0 45135               LDI LIES         IN RIPPLE TEST    1

43357  0074 00 4 00106               TSX OK,4         CONTINUE TEST.
43360  0020 00 0 43326               TRA RSI1         REPEAT TEST.
```

RIPPLE TEST- CHECKING OAI AND OSI.

EACH COL CHECKED INDIVIDUALLY.

WITH XRA CHECKING
2 OAI
1 OSI

```
43361  002131006231              BCD 10AI0SI
43362  0074 00 4 45152   RSI2    TSX  CLEAR,4
43363  0774 00 1 00002           AXT 2,1          FOR XEC
43364  0774 00 2 00044           AXT 36,2         STEP COUNT.
43365 -0500 00 0 45114           CAL BIT35
43366  0602 00 0 45135           SLW LIES         SAVE.
43367 -0500 00 0 45135           CAL LIES
43370  0441 00 0 45100           LDI BZERO

43371  0522 00 1 43414           XEC RSI2A+2,1 XEC OAI OR OSI

43372  0604 00 0 45136           STI LIES+1
43373  0500 00 0 45136           CLA LIES+1
43374  0340 00 0 45135           CAS LIES
43375  0020 00 0 43377           TRA *+2          ERROR-
43376  0020 00 0 43405           TRA RSI2B        OK-  TRY AGAIN.

43377  0760 00 0 00161           SWT 1            WANT A CLOSED LOOP...
43400  0020 00 0 43402           TRA *+2          UP-  NO  -GO ON.
43401  0020 00 0 43367           TRA RSI2+5       DN- YES  -REPEAT SAME VAL.

43402  0560 00 0 45135           LDQ LIES
43403  0074 00 4 00104           TSX ERROR-1,4
43404  0020 00 0 43362           TRA RSI2


43405 -0500 00 0 45135   RSI2B CAL LIES         STEPPING BIT
43406  0767 00 0 00001           ALS 1              ONE COLUMN.
43407  2 00001 2 43366           TIX RSI2+4,2,1 KEEPING COUNT.

43410  2 00001 1 43364           TIX RSI2+2,1,1 REPEAT FOR OSI
43411  0020 00 0 43414           TRA *+3          JUMP OVER SEC LOC


                                                                    XRA
43412  0043 00 0 00000   RSI2A OAI              TWO INST IN          2
43413  0442 00 0 45135         OSI LIES        RIPPLE TEST.         1
43414  0074 00 4 00106         TSX OK,4        CONTINUE TEST.
43415  0020 00 0 43362         TRA RSI2        REPEAT TEST.
```

S E C T I O N T H R E E

```
          RIPPLE TEST - CHECKING IIA AND IIS
                                EACH COL CHECKED INDIVIDUALLY.
                                BIT INV FROM 0 TO 1.
          WITH XRA     CHECKING
                2          IIA
                1          IIS

43416  313121313162              BCD 1IIAIIS
43417  0074 00 4 45152    RSI3   TSX  CLEAR,4
43420  0774 00 1 00002           AXT 2,1         FOR XEC
43421  0774 00 2 00044           AXT 36,2        STEP COUNT
43422 -0500 00 0 45114           CAL BIT35
43423  0602 00 0 45135           SLW LIES
43424 -0500 00 0 45135           CAL LIES
43425  0441 00 0 45100           LDI BZERO

43426  0522 00 1 43451           XEC RSI3A+2,1 XEC IIA OR IIS.

43427  0604 00 0 45136           STI LIES+1
43430  0500 00 0 45136           CLA LIES+1
43431  0340 00 0 45135           CAS LIES
43432  0020 00 0 43434           TRA *+2         ERROR
43433  0020 00 0 43442           TRA RSI3B       OK- TRY AGAIN.

43434  0760 00 0 00161           SWT 1           WANT A CLOSED LOOP...
43435  0020 00 0 43437           TRA *+2         UP -  NO  -GO ON
43436  0020 00 0 43424           TRA RSI3+5      DN - YES  -REPEAT SAME VAL

43437  0560 00 0 45135           LDQ LIES
43440  0074 00 4 00104           TSX ERROR-1,4
43441  0020 00 0 43417           TRA RSI3

43442 -0500 00 0 45135    RSI3B  CAL LIES        STEPPING BIT
43443  0767 00 0 00001           ALS 1             ONE COLUMN.
43444  2 00001 2 43423           TIX RSI3+4,2,1  KEEPING COUNT.

43445  2 00001 1 43421           TIX RSI3+2,1,1 REPEAT FOR IIS.
43446  0020 00 0 43451           TRA *+3         JUMP OVER SEC INST.


43447  0041 00 0 00000    RSI3A  IIA             TWO INST IN
43450  0440 00  045135           IIS LIES        RIPPLE TEST.


43451  0074 00 4 00106           TSX OK,4
43452  0020 00 0 43417           TRA RSI3
```

```
                RIPPLE TEST - CHECKING IIA AND IIS
                                        EACH COL CHECKED INDIVIDUALLY.
                                        BIT INV FROM 1 TO 0.
                WITH XRA     CHECKING
                     2          IIA
                     1          IIS

43453   313121313162                BCD 1IIAIIS
43454   0074 00 4 45152     RSI4    TSX  CLEAR,4
43455   0774 00 1 00002             AXT 2,1          FOR XEC
43456   0774 00 2 00044             AXT 36,2         STEP COUNT
43457  -0500 00 0 45114             CAL BIT35
43460   0602 00 0 45135             SLW LIES
43461  -0500 00 0 45135             CAL LIES
43462   0044 00 0 00000             PAI              SET RESP SI COL.

43463   0522 00 1 43502             XEC RSI4A+2,1    XEC IIA OR IIS.

43464  -0046 00 0 00000             PIA              IND TO ACC FOR CK.
43465   0100 00 0 43473             TZE RSI4B        TRA IF OK.

43466   0760 00 0 00161             SWT 1            WANT A CLOSED LOOP...
43467   0020 00 0 43471             TRA *+2          UP-  NO  -GO ON.
43470   0020 00 0 43461             TRA RSI4+5       DN- YES  -REPEAT SAME VAL.

43471   0074 00 4 00104             TSX ERROR-1,4
43472   0020 00 0 43454             TRA RSI4

43473  -0500 00 0 45135     RSI4B   CAL LIES        STEPPING BIT
43474   0767 00 0 00001             ALS 1              ONE COLUMN.
43475   2 00001 2 43460             TIX RSI4+4,2,1   KEEPING COUNT.

43476   2 00001 1 43456             TIX RSI4+2,1,1 REPEAT FOR IIS
43477   0020 00 0 43502             TRA *+3          JUMP OVER XEC INST.

43500   0041 00 0 00000     RSI4A   IIA              TWO INST IN
43501   0440 00  045135             IIS LIES           RIPPLE TEST


43502   0074 00 4 00106             TSX OK,4         CONTINUE TEST.
43503   0020 00 0 43454             TRA RSI4         REPEAT TEST.
```

S E C T I O N T H R E E

RIPPLE TEST - CHECKING RIA AND RIS.

WITH XRA CHECKING
2 RIA
1 RIS

```
43504  513121513162            BCD 1RIARIS
43505  0074 00 4 45152   RSI5  TSX  CLEAR,4
43506  0774 00 1 00002         AXT 2,1         FOR XEC
43507  0774 00 2 00044         AXT 36,2        STEP COUNT
43510 -0500 00 0 45114         CAL BIT35
43511  0602 00 0 45135         SLW LIES
43512 -0500 00 0 45135         CAL LIES
43513  0044 00 0 00000         PAI             SET RESP SI COL.

43514  0522 00 1 43533         XEC RSI5A+2,1 XEC RIA OR RIS.

43515 -0046 00 0 00000         PIA             IND TO ACC FOR CK.
43516  0100 00 0 43524         TZE RSI5B       TRA IF OK.

43517  0760 00 0 00161         SWT 1           WANT A CLOSED LOOP...
43520  0020 00 0 43522         TRA *+2         UP-  NO  -GO ON.
43521  0020 00 0 43512         TRA RSI5+5      DN- YES  -REPEAT SAME VAL.

43522  0074 00 4 00104         TSX ERROR-1,4
43523  0020 00 0 43505         TRA RSI5

43524 -0500 00 0 45135   RSI5B CAL LIES        STEPPING BIT
43525  0767 00 0 00001         ALS 1             ONE COLUMN.
43526  2 00001 2 43511         TIX RSI5+4,2,1 KEEPING COUNT.

43527  2 00001 1 43507         TIX RSI5+2,1,1 REPEAT FOR RIS.
43530  0020 00 0 43533         TRA *+3         JUMP OVER XEC INST.

43531 -0042 00 0 00000   RSI5A RIA             TWO INST IN
43532  0445 00 0 45135         RIS LIES          RIPPLE TEST.


43533  0074 00 4 00106         TSX OK,4        CONTINUE TEST.
43534  0020 00 0 43505         TRA RSI5        REPEAT TEST.
```

RIPPLE TEST - CHECKING SIR AND IIR
FOR IIR, INV 0 TO 1.

WITH XRA CHECKING
2 SIR
1 SIL

```
43535  623151313151            BCD 1SIRIIR
43536  0074 00 4 45152   RSI6  TSX  CLEAR,4
43537  0774 00 1 00002         AXT 2,1        FOR XEC
43540  0774 00 2 00022         AXT 18,2       STEP COUNT
43541 -0500 00 0 45114         CAL BIT35
43542  0602 00 0 45135         SLW LIES
43543 -0500 00 0 45135         CAL LIES
43544  0621 00 1 43572         STA RSI6A+2,1
43545  0625 00 1 43572         STT RSI6A+2,1
43546  0441 00 0 45100         LDI BZERO      CLEAR SI REG.

43547  0522 00 1 43572         XEC RSI6A+2,1  XEC SIR OR IIR

43550  0604 00 0 45136         STI LIES+1
43551  0500 00 0 45136         CLA LIES+1
43552  0340 00 0 45135         CAS LIES
43553  0020 00 0 43555         TRA *+2        ERROR
43554  0020 00 0 43563         TRA RSI6B      OK-  TRY AGAIN.

43555  0760 00 0 00161         SWT 1          WANT A CLOSED LOOP...
43556  0020 00 0 43560         TRA *+2        UP-  NO  -GO ON.
43557  0020 00 0 43543         TRA RSI6+5     DN- YES  -REPEAT SAME VAL.

43560  0560 00 0 45135         LDQ LIES       CORR RESULT
43561  0074 00 4 00104         TSX ERROR-1,4
43562  0020 00 0 43536         TRA RSI6

43563 -0500 00 0 45135   RSI6B CAL LIES       STEPPING BIT
43564  0767 00 0 00001         ALS 1            ONE COLUMN.
43565  2 00001 2 43542         TIX RSI6+4,2,1 KEEPING COUNT.

43566  2 00001 1 43540         TIX RSI6+2,1,1 REPEAT FOR IIR.
43567  0020 00 0 43572         TRA *+3        JUMP OVER XEC INSTS.

43570  0055 00  000000  RSI6A SIR **          TWO INST IN
43571  0051 00  000000         IIR **           RIPPLE TEST.


43572  0074 00 4 00106         TSX OK,4       CONTINUE TEST.
43573  0020 00 0 43536         TRA RSI6       REPEAT TEST.
```

RIPPLE TEST - CHECKING RIR AND IIR
FOR IIR, INV 1 TO 0.

WITH XRA 2 CHECKING RIR
1 IIR

```
43574  513151313151            BCD 1RIRIIR
43575  0074 00 4 45152   RSI7  TSX  CLEAR,4
43576  0774 00 1 00002         AXT 2,1          FOR XEC
43577  0774 00 2 00022         AXT 18,2         STEP COUNT
43600 -0500 00 0 45114         CAL BIT35
43601  0602 00 0 45135         SLW LIES
43602 -0500 00 0 45135         CAL LIES
43603  0621 00 1 43626         STA RSI7A+2,1
43604  0625 00 1 43626         STT RSI7A+2,1
43605  0044 00 0 00000         PAI              SET RESP SI COL.

43606  0522 00 1 43626         XEC RSI7A+2,1    XEC RIR OR IIR

43607 -0046 00 0 00000         PIA              IND TO ACC FOR CK.
43610  0100 00 0 43617         TZE RSI7B        TRA, IF OK.

43611  0760 00 0 00161         SWT 1            WANT A CLOSED LOOP...
43612  0020 00 0 43614         TRA *+2          UP-  NO  -GO ON.
43613  0020 00 0 43602         TRA RSI7+5       DN- YES  -REPEAT SAME VAL.

43614  0560 00 0 45135         LDQ LIES
43615  0074 00 4 00104         TSX ERROR-1,4
43616  0020 00 0 43575         TRA RSI7

43617 -0500 00 0 45135  RSI7B  CAL LIES         STEP BIT
43620  0767 00 0 00001         ALS 1              ONE COLUMN.
43621  2 00001 2 43601         TIX RSI7+4,2,1   KEEPING COUNT.

43622  2 00001 1 43577         TIX RSI7+2,1,1   REPEAT FOR IIR.
43623  0020 00 0 43626         TRA *+3          JUMP OVER XEC INST.

43624  0057 00  000000  RSI7A  RIR **           TWO INST IN
43625  0051 00  000000         IIR **             RIPPLE TEST.


43626  0074 00 4 00106         TSX OK,4         CONTINUE TEST.
43627  0020 00 0 43575         TRA RSI7         REPEAT TEST.
```

RIPPLE TEST - CHECKING SIL AND IIL
FOR IIL, INV 0 TO 1.

WITH XRA 2 CHECKING SIL
1 IIL

```
43630  623143313143            BCD 1SILIIL
43631  0074 00 4 45152   RSI8  TSX  CLEAR,4
43632  0774 00 1 00002         AXT 2,1        FOR XEC
43633  0774 00 2 00022         AXT 18,2       STEP COUNT
43634 -0500 00 0 45114         CAL BIT35
43635  0602 00 0 45135         SLW LIES
43636 -0500 00 0 45135         CAL LIES
43637  0621 00 1 43667         STA RSI8A+2,1
43640  0625 00 1 43667         STT RSI8A+2,1
43641  0767 00 0 00022         ALS 18
43642  0602 00 0 45136         SLW LIES+1
43643  0441 00 0 45100         LDI BZERO      CLEAR SI REG.

43644  0522 00 1 43667         XEC RSI8A+2,1 XEC SIL OR IIL

43645  0604 00 0 45137         STI LIES+2
43646  0500 00 0 45137         CLA LIES+2
43647  0340 00 0 45136         CAS LIES+1
43650  0020 00 0 43652         TRA *+2        ERROR
43651  0020 00 0 43660         TRA RSI8B      OK-  TRY AGAIN.

43652  0760 00 0 00161         SWT 1          WANT A CLOSED LOOP...
43653  0020 00 0 43655         TRA *+2        UP-  NO  -GO ON.
43654  0020 00 0 43636         TRA RSI8+5     DN- YES  -REPEAT SAME VAL.

43655  0560 00 0 45136         LDQ LIES+1
43656  0074 00 4 00104         TSX ERROR-1,4
43657  0020 00 0 43631         TRA RSI8

43660 -0500 00 0 45135   RSI8B CAL LIES       STEPPING BIT
43661  0767 00 0 00001         ALS 1            ONE COLUMN.
43662  2 00001 2 43635         TIX RSI8+4,2,1 KEEPING COUNT.

43663  2 00001 1 43633         TIX RSI8+2,1,1 REPEAT FOR IIL.
43664  0020 00 0 43667         TRA *+3


43665 -0055 00  000000   RSI8A SIL **         TWO INST USED
43666 -0051 00  000000         IIL **           IN RIPPLE TEST.


43667  0074 00 4 00106         TSX OK,4       CONTINUE TEST.
43670  0020 00 0 43631         TRA RSI8       REPEAT TEST.
```

SECTION THREE

RIPPLE TEST - CHECKING RIL AND IIL

FOR IIL, INV 1 TO 0.

```
          WITH XRA     CHECKING
                2          RIL
                1          IIL

43671   513143313143              BCD 1RILIIL
43672   0074 00 4 45152   RSI9    TSX  CLEAR,4
43673   0774 00 1 00002           AXT 2,1          FOR XEC
43674   0774 00 2 00022           AXT 18,2         STEP COUNT
43675  -0500 00 0 45114           CAL BIT35
43676   0602 00 0 45135           SLW LIES
43677  -0500 00 0 45135           CAL LIES
43700   0621 00 1 43725           STA RSI9A+2,1
43701   0625 00 1 43725           STT RSI9A+2,1
43702   0767 00 0 00022           ALS 18
43703   0044 00 0 00000           PAI              SET RESP SI COL.
43704   0602 00 0 45136           SLW LIES+1

43705   0522 00 1 43725           XEC RSI9A+2,1 XEC RIL OR IIL.

43706  -0046 00 0 00000           PIA              IND TO ACC FOR CK.
43707   0100 00 0 43716           TZE RSI9B        TRA, IF OK.

43710   0760 00 0 00161           SWT 1            WANT A CLOSED LOOP...
43711   0020 00 0 43713           TRA *+2          UP-  NO  -GO ON.
43712   0020 00 0 43677           TRA RSI9+5       DN-  YES -REPEAT SAME VAL

43713   0560 00 0 45136           LDQ LIES+1
43714   0074 00 4 00104           TSX ERROR-1,4
43715   0020 00 0 43672           TRA RSI9

43716  -0500 00 0 45135   RSI9B   CAL LIES         STEP BIT
43717   0767 00 0 00001           ALS 1              ONE COLUMN.
43720   2 00001 2 43676           TIX RSI9+4,2,1 KEEPING COUNT.

43721   2 00001 1 43674           TIX RSI9+2,1,1 REPEAT FOR IIL
43722   0020 00 0 43725           TRA *+3          JUMP OVER XEC INST.


43723  -0057 00  000000   RSI9A   RIL **           TWO INST USED
43724  -0051 00  000000           IIL **             IN RIPPLE TEST.


43725   0074 00 4 00106           TSX OK,4         CONTINUE TEST.
43726   0020 00 0 43672           TRA RSI9         REPEAT TEST.
```

```
                CHECKING SI TO NOT ALTER CONT OF ACC
                                        ACC SET TO ALL ZEROES.
43727  212323234260                BCD 1ACCCK
43730  0074 00 4 45152    SIA1     TSX  CLEAR,4
43731  0774 00 1 00012             AXT 10,1        FOR XEC INST
43732 -0754 00 0 00000             PXD             CLEAR ACC

43733  0522 00 1 43775             XEC SIA1A+10,1 XEC 10 SI INST

43734 -0100 00 0 43736             TNZ *+2         TRA ON ERROR.
43735  0120 00 0 43740             TPL *+3         TRA, IF OK.
43736  0074 00 4 00104             TSX ERROR-1,4
43737  0020 00 0 43730             TRA SIA1

43740  2 00001 1 43732             TIX SIA1+2,1,1 STEP TO NEXT INST
43741  0074 00 4 00106    SIA1B    TSX OK,4        CONTINUE TEST
43742  0020 00 0 43730             TRA SIA1        REPEAT TEST


                CHECKING SI INST TO NOT ALTER CONT OF ACC
                                        ACC SET TO ALL ONES.
43743  212323234260                BCD 1ACCCK
43744  0074 00 4 45152    SIA2     TSX  CLEAR,4
43745  0774 00 1 00012             AXT 10,1
43746 -0754 00 0 00000             PXD             CLEAR ACC
43747  0760 00 0 00006             COM             1S - Q,P,1-35
43750 -0760 00 0 00003             SSM             1 TO S

43751  0522 00 1 43775             XEC SIA1A+10,1 XEC 10 SI INST.

43752  0760 00 0 00006             COM
43753  0760 00 0 00002             CHS
43754  0560 00 0 45101             LDQ BS135
43755 -0100 00 0 43757             TNZ *+2         TRA ON ERROR.
43756  0120 00 0 43761             TPL *+3         TRA, IF OK.
43757  0074 00 4 00104             TSX ERROR-1,4
43760  0020 00 0 43744             TRA SIA2

43761  2 00001 1 43746             TIX SIA2+2,1,1
43762  0020 00 0 43775             TRA SIA2B       JUMP OVER THE XEC INSTS.

                              CHECKING          WITH                XRA
43763  0044 00 0 00000    SIA1A PAI             10 SI               12
43764  0043 00 0 00000          OAI              INST                11
43765 -0042 00 0 00000          RIA               USED               10
43766  0041 00 0 00000          IIA                IN                 7
43767  0055 00  000000          SIR                 ACC               6
43770 -0055 00  000000          SIL                  CHECK.           5
43771  0057 00  000000          RIR                                   4
43772 -0057 00  000000          RIL                                   3
43773  0051 00  000000          IIR                                   2
43774 -0051 00  000000          IIL                                   1

43775  0074 00 4 00106    SIA2B TSX OK,4
43776  0020 00 0 43744          TRA SIA2
```

S E C T I O N T H R E E

CHECKING SI INST TO NOT ALTER CONT OF STORAGE
STORAGE EITHER ALL ZEROES OR ALL ONES.

```
43777  626346512342              BCD 1STORCK
44000  0074 00 4 45152   SIA3    TSX  CLEAR,4
44001  0774 00 1 00002           AXT 2,1
44002  0774 00 2 00006           AXT 6,2
44003 -0500 00 1 45102           CAL BZERO+2,1 XRA 2 - LOAD ZEROES.
                                               XRA 1 - LOAD ONES.
44004  0602 00 0 45135           SLW LIES

44005  0522 00 2 44027           XEC SIA3A+6,2
44006  0761 00 0 00000           NOP           FOR SKIP INST.

44007  0500 00 0 45135           CLA LIES
44010  0340 00 1 45102           CAS BZERO+2,1
44011  0020 00 0 44013           TRA *+2       ERROR
44012  0020 00 0 44016           TRA *+4       OK-TRY AGAIN.
44013  0560 00 1 45102           LDQ BZERO+2,1
44014  0074 00 4 00104           TSX ERROR-1,4
44015  0020 00 0 44000           TRA SIA3

44016  2 00001 2 44003           TIX SIA3+3,2,1 STEP TO NEXT SI INST.

44017  2 00001 1 44002           TIX SIA3+2,1,1 REPEAT FOR ALL ONES.
44020  0020 00 0 44027           TRA SIA3B

                                 CHECKING              WITH          XRB
44021  0441 00 0 45135   SIA3A LDI LIES                              6
44022  0442 00 0 45135         OSI LIES                              5
44023  0440 00  045135         IIS LIES                              4
44024  0445 00 0 45135         RIS LIES                              3
44025  0444 00 0 45135         OFT LIES                              2
44026  0446 00 0 45135         ONT LIES                              1

44027  0074 00 4 00106   SIA3B TSX OK,4       CONTINUE TEST
44030  0020 00 0 44000         TRA SIA3       REPEAT TEST
```

CHECKING TRA OR SKIP SI INST TO NOT ALTER CONT SI REG
SI REG EITHER SET TO ALL ZEROES OR ALL ONES.

```
44031  623160234260            BCD 1SI CK
44032  0074 00 4 45152   SIA4  TSX  CLEAR,4
44033  0774 00 1 00002         AXT 2,1
44034  0774 00 2 00010         AXT 8,2
44035 -0500 00 0 45100         CAL BZERO
44036  0441 00 1 45102         LDI BZERO+2,1 XRA 2 - LOAD ZEROES.
                                             XRA 1 - LOAD ONES.

44037  0522 00 2 44064         XEC SIA4A+8,2
44040  0761 00 0 00000         NOP           FOR SKIP INST

44041  0604 00 0 45135   SIA4B STI LIES
44042  0500 00 0 45135         CLA LIES
44043  0340 00 1 45102         CAS BZERO+2,1
44044  0020 00 0 44046         TRA *+2       ERROR
44045  0020 00 0 44051         TRA *+4       OK-TRY AGAIN.
44046  0560 00 1 45102         LDQ BZERO+2,1
44047  0074 00 4 00104         TSX ERROR-1,4
44050  0020 00 0 44032         TRA SIA4

44051  2 00001 2 44035         TIX SIA4+3,2,1 STEP TO NEXT SI INST.

44052  2 00001 1 44034         TIX SIA4+2,1,1 REPEAT FOR ALL ONES.
44053  0020 00 0 44064         TRA SIA4C

                          CHECKING          WITH                XRB
44054  0446 00 0 00000   SIA4A ONT                                10
44055  0444 00 0 00000         OFT                               7
44056  0054 00  000000         RFT                               6
44057  0056 00  000000         RNT                               5
44060 -0054 00  000000         LFT                               4
44061 -0056 00  000000         LNT                               3
44062  0042 00 0 44041         TIO SIA4B                         2
44063  0046 00 0 44041         TIF SIA4B                         1

44064  0074 00 4 00106   SIA4C TSX OK,4
44065  0020 00 0 44032         TRA SIA4
```

```
                CHECKING Q BIT TO NOT SET SI REG

44066   502551516060                BCD 1QERR
44067   0074 00 4 45152     SIQ     TSX  CLEAR,4
44070   0774 00 1 00003             AXT 3,1          LOAD XRA FOR XEC
44071   0441 00 0 45100             LDI BZERO
44072  -0500 00 0 45112             CAL BIT1         PLACE BIT IN
44073   0767 00 0 00003             ALS 3               COLUMN Q.

44074   0522 00 1 44106             XEC SIQA+3,1     XEC 3 SI INST

44075  -0046 00 0 00000             PIA              IND TO ACC FOR CK
44076   0100 00 0 44101             TZE *+3
44077   0074 00 4 00104             TSX ERROR-1,4    ERROR
44100   0020 00 0 44067             TRA SIQ

44101   2 00001 1 44071             TIX SIQ+2,1,1    STEP TO NEXT INST.
44102   0020 00 0 44106             TRA SIQB

                                CHECKING            WITH                XRA
44103   0044 00 0 00000     SIQA    PAI                                     3
44104   0043 00 0 00000             OAI                                     2
44105   0041 00 0 00000             IIA                                     1

44106   0074 00 4 00106     SIQB    TSX OK,4         CONTINUE TEST.
44107   0020 00 0 44067             TRA SIQ          REPEAT TEST.

                CHECKING S BIT TO NOT SET SI REG

44110   622551516060                BCD 1SERR
44111   0074 00 4 45152     SIS     TSX  CLEAR,4
44112   0774 00 1 00003             AXT 3,1
44113  -0754 00 0 00000             PXD              CLEAR ACC
44114  -0760 00 0 00003             SSM

44115   0522 00 1 44106             XEC SIQA+3,1

44116  -0046 00 0 00000             PIA              IND TO ACC FOR CK.
44117   0100 00 0 44123             TZE *+4
44120   0074 00 4 00104             TSX ERROR-1,4    ERROR
44121   0020 00 0 44111             TRA SIS

44122   2 00001 1 44113             TIX SIS+2,1,1    STEP TO NEXT INST

44123   0074 00 4 00106             TSX OK,4         CONTINUE TEST
44124   0020 00 0 44111             TRA SIS          REPEAT TEST
```

CHECKING PAI, PIA, AND STI FOR RELIABILITY

```
44125   636231220160                BCD 1TSIB1
44126   0074 00 4 45152     SIB1    TSX  CLEAR,4
44127  -0500 00 0 45121             CAL SIBP1       L 765432112345
44130   0044 00 0 00000             PAI
44131   0604 00 0 45135             STI LIES
44132  -0754 00 0 00000             PXD             CLEAR ACC
44133  -0046 00 0 00000             PIA
44134   0602 00 0 45136             SLW LIES+1
44135   0500 00 0 45136             CLA LIES+1
44136   0340 00 0 45135             CAS LIES
44137   0020 00 0 44141             TRA *+2         ERROR
44140   0020 00 0 44143             TRA *+3         OK-  GO ON.
44141   0560 00 0 45121             LDQ SIBP1
44142   0074 00 4 00105             TSX ERROR,4
44143   0074 00 4 00106             TSX OK,4        CONTINUE TEST.
44144   0020 00 0 44126             TRA SIB1        REPEAT TEST.
```

S E C T I O N T H R E E

CHECKING LDI AND PAI WITH VARIOUS BIT PATTERNS

IN THIS TEST, XRB GOVERNS THE BIT PATTERN.

WITH XRB SET AT, BIT PATTERN IS-

3	111111111111
2	222222222222
1	444444444444

WITH XRA	CHECKING
2	LDI
1	PAI

```
44145   432431472131            BCD 1LDIPAI
44146   0074 00 4 45152   SIB2  TSX  CLEAR,4
44147   0774 00 1 00002         AXT 2,1         FOR XEC
44150   0774 00 2 00003         AXT 3,2         FOR BIT PATTERN.
44151  -0500 00 2 45120         CAL P01S+3,2

44152   0522 00 1 44173         XEC SIB2A+2,1 XEC LDI OR PAI.

44153   0604 00 0 45135         STI LIES
44154   0500 00 0 45135         CLA LIES
44155   0560 00 2 45120         LDQ P01S+3,2  FOR ERROR PRINTOUT.
44156   0340 00 2 45120         CAS P01S+3,2
44157   0020 00 0 44161         TRA *+2         ERROR
44160   0020 00 0 44166         TRA SIB2B       OK-TRY AGAIN.

44161   0760 00 0 00161         SWT 1           WANT A CLOSED LOOP...
44162   0020 00 0 44164         TRA *+2         UP-  NO  -GO ON.
44163   0020 00 0 44151         TRA SIB2+3      DN- YES  -REP SAME VAL.

44164   0074 00 4 00104         TSX ERROR-1,4
44165   0020 00 0 44146         TRA SIB2

44166   2 00001 2 44151   SIB2B TIX SIB2+3,2,1 REP WITH ANOTHER BIT PATT.

44167   2 00001 1 44150         TIX SIB2+2,1,1 REP FOR PAI
44170   0020 00 0 44173         TRA SIB2C


44171   0441 00 2 45120   SIB2A LDI P01S+3,2
44172   0044 00 0 00000         PAI


44173   0074 00 4 00106   SIB2C TSX OK,4       CONTINUE TEST.
44174   0020 00 0 44146         TRA SIB2        REPEAT TEST.
```

CHECKING OSI AND OAI WITH VARIOUS BIT PATTERNS

IN THIS TEST, XRB GOVERNS THE BIT PATTERN.
WITH XRB SET AT, BIT PATTERN IS-

3	111111111111
2	222222222222
1	444444444444

WITH XRA CHECKING

2	OSI
1	OAI

```
44175  466231462131              BCD 10SI0AI
44176  0074 00 4 45152    SIB3   TSX  CLEAR,4
44177  0774 00 1 00002           AXT 2,1        FOR XEC
44200  0441 00 0 45100           LDI BZERO      INITIALIZE.
44201  0774 00 2 00003           AXT 3,2        FOR BIT PATT SELECTION.

44202 -0500 00 2 45120           CAL P01S+3,2

44203  0522 00 1 44224           XEC SIB3A+2,1 XEC OSI OR OAI.

44204  0604 00 0 45135           STI LIES
44205  0500 00 0 45135           CLA LIES
44206  0560 00 2 44227           LDQ SIB3A+5,2 FOR ERROR PRINTOUT.
44207  0340 00 2 44227           CAS SIB3A+5,2
44210  0020 00 0 44212           TRA *+2        ERROR
44211  0020 00 0 44217           TRA SIB3B      OK-TRY AGAIN

44212  0760 00 0 00161           SWT 1          WANT A CLOSED LOOP...
44213  0020 00 0 44215           TRA *+2        UP-  NO  -GO ON.
44214  0020 00 0 44201           TRA SIB3+3     DN- YES  -REP SAME VAL.

44215  0074 00 4 00104           TSX ERROR-1,4
44216  0020 00 0 44176           TRA SIB3

44217  2 00001 2 44202    SIB3B  TIX SIB3+4,2,1 REP WITH ANOTHER BIT PATT.

44220  2 00001 1 44200           TIX SIB3+2,1,1 REP FOR OAI
44221  0020 00 0 44227           TRA SIB3C


44222  0442 00 2 45120    SIB3A  OSI P01S+3,2
44223  0043 00 0 00000           OAI

44224 +111111111111              OCT 111111111111
44225 +333333333333              OCT 333333333333
44226 -377777777777              OCT 777777777777


44227  0074 00 4 00106    SIB3C  TSX OK,4        CONTINUE TEST
44230  0020 00 0 44176           TRA SIB3       REPEAT TEST
```

CHECKING SIL AND SIR WITH VARIOUS BIT PATTERNS

IN THIS TEST, XRB GOVERNS THE BIT PATTERN.
WITH XRB SET AT, BIT PATTERN IS-

3	111111111111
2	222222222222
1	444444444444

```
44231  623143623151            BCD 1SILSIR
44232  0074 00 4 45152   SIB4  TSX CLEAR,4
44233  0774 00 2 00003         AXT 3,2        FOR BIT PATT SEL

44234  0441 00 0 45100         LDI BZERO
44235 -0500 00 2 45120         CAL P01S+3,2
44236  0621 00 0 44242         STA *+4
44237  0621 00 0 44243         STA *+4
44240  0625 00 0 44242         STT *+2
44241  0625 00 0 44243         STT *+2

44242 -0055 00  000000         SIL **
44243  0055 00  000000         SIR **
44244  0604 00 0 45135         STI LIES
44245  0500 00 0 45135         CLA LIES
44246  0560 00 2 44227         LDQ SIB3A+5,2 FOR ERR PRINTOUT.
44247  0340 00 2 44227         CAS SIB3A+5,2
44250  0020 00 0 44252         TRA *+2        ERROR
44251  0020 00 0 44257         TRA SIB4B      OK-TRY AGAIN.

44252  0760 00 0 00161         SWT 1          WANT A CLOSED LOOP...
44253  0020 00 0 44255         TRA *+2        UP-  NO  -GO ON.
44254  0020 00 0 44234         TRA SIB4+2     DN- YES  -REP SAME VAL

44255  0074 00 4 00104         TSX ERROR-1,4
44256  0020 00 0 44232         TRA SIB4

44257  2 00001 2 44235   SIB4B TIX SIB4+3,2,1 REP WITH ANOTHER BIT PATT.
44260  0074 00 4 00106         TSX OK,4       CONTINUE TEST.
44261  0020 00 0 44232         TRA SIB4       REPEAT TEST.
```

CHECKING INVERT SI INST FOR RELIABILITY

IIA IIS IIR IIL

```
44262  314565632342            BCD 1INVTCK
44263  0074 00 4 45152   SIB5  TSX  CLEAR,4
44264  0441 00 0 45100         LDI BZERO      INITIALIZE.
44265 -0500 00 0 45101         CAL BS135
44266  0041 00 0 00000         IIA
44267  0041 00 0 00000         IIA
44270  0041 00 0 00000         IIA
44271  0041 00 0 00000         IIA
44272  0041 00 0 00000         IIA
44273  0041 00 0 00000         IIA
44274  0074 00 2 44326         TSX SIB5A,2    CK RESULTS
44275  0441 00 0 45100         LDI BZERO      INITIALIZE
44276  0440 00  045101         IIS BS135
44277  0440 00  045101         IIS BS135
44300  0440 00  045101         IIS BS135
44301  0440 00  045101         IIS BS135
44302  0440 00  045101         IIS BS135
44303  0440 00  045101         IIS BS135
44304  0074 00 2 44326         TSX SIB5A,2    CK RESULTS
44305  0441 00 0 45100         LDI BZERO      INITIALIZE
44306  0051 00  777777         IIR 777777
44307  0051 00  777777         IIR 777777
44310  0051 00  777777         IIR 777777
44311  0051 00  777777         IIR 777777
44312  0051 00  777777         IIR 777777
44313  0051 00  777777         IIR 777777
44314  0074 00 2 44326         TSX SIB5A,2    CK RESULTS
44315  0441 00 0 45100         LDI BZERO      INITIALIZE
44316 -0051 00  777777         IIL 777777
44317 -0051 00  777777         IIL 777777
44320 -0051 00  777777         IIL 777777
44321 -0051 00  777777         IIL 777777
44322 -0051 00  777777         IIL 777777
44323 -0051 00  777777         IIL 777777
44324  0074 00 2 44326         TSX SIB5A,2    CK RESULTS
44325  0020 00 0 44340         TRA SIB5B      ALL THROUGH

44326 -0046 00 0 00000  SIB5A PIA
44327  0100 00 2 00001         TZE 1,2        OK- GO ON.

44330  0760 00 0 00161         SWT 1          WANT A CLOSED LOOP...
44331  0020 00 0 44333         TRA *+2        UP-  NO  -GO ON.
44332  0020 00 2 77770         TRA -8,2       DN- YES  -REP SAME VAL.

44333 -0634 00 1 45136         SXD LIES+1,1   TO INDICATE ERROR
44334 -0535 00 1 45136         LDC LIES+1,1      ADDR IN XRA.
44335  0074 00 4 00104         TSX ERROR-1,4
44336  0020 00 0 44263         TRA SIB5
44337  0020 00 2 00001         TRA 1,2
44340  0074 00 4 00106  SIB5B TSX OK,4        CONTINUE TEST
44341  0020 00 0 44263         TRA SIB5       REPEAT TEST
```

CHECKING INV SI INST WITH VARIOUS BIT PATTERNS

```
44342   314565632342              BCD 1INVTCK
44343   0074 00 4 45152    SIB6   TSX  CLEAR,4
44344  -0500 00 0 45110           CAL P52S        BIT PATT  101  010
44345   0441 00 0 45100           LDI BZERO         CONT OF SI REG SHOULD BE-
44346   0041 00 0 00000           IIA                       525252525252
44347   0440 00  045107           IIS P25S                  777777777777
44350   0051 00  252525           IIR 252525                777777525252
44351  -0051 00  252525           IIL 252525                525252525252
44352   0041 00 0 00000           IIA                       000000000000
44353   0440 00  045101           IIS BS135                 777777777777
44354   0051 00  112345           IIR 112345                777777665432
44355  -0051 00  765432           IIL 765432                012345665432
44356   0440 00  045121           IIS SIBP1                 777777777777
44357   0041 00 0 00000           IIA                       252525252525
44360   0440 00  045101           IIS BS135                 525252525252
44361   0041 00 0 00000           IIA                       000000000000
44362   0041 00 0 00000           IIA                       525252525252
44363   0440 00  045107           IIS P25S                  777777777777
44364   0051 00  252525           IIR 252525                777777525252
44365  -0051 00  252525           IIL 252525                525252525252
44366   0041 00 0 00000           IIA                       000000000000
44367   0440 00  045101           IIS BS135                 777777777777
44370   0051 00  112345           IIR 112345                777777665432
44371  -0051 00  765432           IIL 765432                012345665432
44372   0440 00  045121           IIS SIBP1                 777777777777
44373   0041 00 0 00000           IIA                       252525252525
44374   0440 00  045101           IIS BS135                 525252525252
44375   0041 00 0 00000           IIA                       000000000000
44376   0041 00 0 00000           IIA                       525252525252
44377   0440 00  045107           IIS P25S                  777777777777
44400   0051 00  252525           IIR 252525                777777525252
44401  -0051 00  252525           IIL 252525                525252525252
44402   0041 00 0 00000           IIA                       000000000000
44403   0440 00  045101           IIS BS135                 777777777777
44404   0051 00  112345           IIR 112345                777777665432
44405  -0051 00  765432           IIL 765432                012345665432
44406   0440 00  045121           IIS SIBP1                 777777777777
44407   0041 00 0 00000           IIA                       252525252525
44410   0440 00  045101           IIS BS135                 525252525252
44411   0041 00 0 00000           IIA                       000000000000

44412  -0046 00 0 00000           PIA             INDICATORS TO ACC FOR CHECK
44413   0100 00 0 44415           TZE *+2
44414   0074 00 4 00105           TSX ERROR,4
44415   0074 00 4 00106           TSX OK,4        CONTINUE TEST
44416   0020 00 0 44343           TRA SIB6        REPEAT TEST
```

CHECKING RIA AND RIS WITH VARIOUS BIT PATTERNS

IN THIS TEST, XRB GOVERNS THE BIT PATTERN.
WITH XRB SET AT, BIT PATT IS-

3	111111111111
2	222222222222
1	444444444444

WITH XRA	CHECKING
2	RIA
1	RIS

```
44417  513121513162             BCD 1RIARIS
44420  0074 00 4 45152   SIB7   TSX  CLEAR,4
44421  0774 00 1 00002          AXT 2,1          FOR XEC
44422  0774 00 2 00003          AXT 3,2          FOR VARIOUS BIT PATT.
44423 -0500 00 2 45120          CAL P01S+3,2
44424  0441 00 0 45101          LDI BS135

44425  0522 00 1 44446          XEC SIB7A+2,1 XEC RIA OR RIS

44426  0604 00 0 45135          STI LIES
44427  0500 00 0 45135          CLA LIES
44430  0560 00 0 45135          LDQ LIES
44431  0340 00 2 44451          CAS SIB7A+5,2
44432  0020 00 0 44434          TRA *+2          ERROR
44433  0020 00 0 44451          TRA SIB7B        OK- TRY AGAIN.

44434  0760 00 0 00161          SWT 1            WANT A CLOSED LOOP...
44435  0020 00 0 44437          TRA *+2          UP-  NO  -GO ON.
44436  0020 00 0 44423          TRA SIB7+3       DN- YES  -REP SAME VAL.

44437  0074 00 4 00104          TSX ERROR-1,4
44440  0020 00 0 44420          TRA SIB7

44441  2 00001 2 44423          TIX SIB7+3,2,1 STEP TO NEXT BIT PATT.

44442  2 00001 1 44422          TIX SIB7+2,1,1 REP FOR RIS
44443  0020 00 0 44451          TRA SIB7B


44444 -0042 00 0 00000   SIB7A RIA
44445  0445 00 2 45120          RIS P01S+3,2
44446 -266666666666             OCT 666666666666 CONTENTS OF SI REG
44447 -155555555555             OCT 555555555555   AFTER EACH
44450 +333333333333             OCT 333333333333     RESET OPERATION.


44451  0074 00 4 00106   SIB7B  TSX OK,4         CONTINUE TEST
44452  0020 00 0 44420          TRA SIB7         REPEAT TEST
```

CHECKING TIF WITH VARIOUS BIT PATTERNS.

```
44453   633126606060            BCD 1TIF
44454   0074 00 4 45152   SIB8  TSX  CLEAR,4
44455   0441 00 0 45115         LDI P01S       BIT PATT  001  001
44456  -0500 00 0 45117         CAL P04S       BIT PATT  100  100
44457   0046 00 0 44462         TIF *+3        SHOULD TRANSFER
44460   0074 00 4 00104         TSX ERROR-1,4
44461   0020 00 0 44454         TRA SIB8

44462  -0500 00 0 45120         CAL P03S       BIT PATT  011  011
44463   0046 00 0 44465         TIF *+2        SHOULDNT TRANSFER
44464   0020 00 0 44467         TRA *+3
44465   0074 00 4 00104         TSX ERROR-1,4
44466   0020 00 0 44454         TRA SIB8

44467  -0500 00 0 45115         CAL P01S       BIT PATT  001  001
44470   0046 00 0 44472         TIF *+2        SHOULDNT TRANSFER
44471   0020 00 0 44473         TRA *+2
44472   0074 00 4 00105         TSX ERROR,4
44473   0074 00 4 00106         TSX OK,4
44474   0020 00 0 44454         TRA SIB8
```

CHECKING TIO WITH VARIOUS BIT PATTERNS.

```
44475   633146606060            BCD 1TIO
44476   0074 00 4 45152   SIB9  TSX  CLEAR,4
44477   0441 00 0 45115         LDI P01S       BIT PATT  001  001
44500  -0500 00 0 45117         CAL P04S       BIT PATT  100  100
44501   0042 00 0 44503         TIO *+2        SHOULDNT TRANSFER
44502   0020 00 0 44505         TRA *+3
44503   0074 00 4 00104         TSX ERROR-1,4
44504   0020 00 0 44476         TRA SIB9

44505  -0500 00 0 45120         CAL P03S       BIT PATT  011  011
44506   0042 00 0 44510         TIO *+2        SHOULDNT TRANSFER
44507   0020 00 0 44512         TRA *+3
44510   0074 00 4 00104         TSX ERROR-1,4
44511   0020 00 0 44476         TRA SIB9

44512  -0500 00 0 45115         CAL P01S       BIT PATT  001  001
44513   0042 00 0 44515         TIO *+2        SHOULD TRANSFER
44514   0074 00 4 00105         TSX ERROR,4
44515   0074 00 4 00106         TSX OK,4
44516   0020 00 0 44476         TRA SIB9
```

RIPPLE TEST - OFT

```
44517  462663606060          BCD 1OFT
44520  0074 00 4 45152  SIB10 TSX  CLEAR,4
44521  0774 00 1 00043       AXT 35,1        EACH COLUMN.
44522 -0500 00 0 45114       CAL BIT35
44523  0602 00 0 45135       SLW LIES
44524 -0500 00 0 45135       CAL LIES
44525  0760 00 0 00006       COM             ALL ONES TO SI REG
44526  0044 00 0 00000       PAI               EXCEPT COLUMN TESTED.
44527  0444 00 0 45135       OFT LIES        SHOULD SKIP
44530  0020 00 0 44532       TRA *+2         ERROR...
44531  0020 00 0 44537       TRA SIB11       TRY AGAIN.

44532  0760 00 0 00161       SWT 1           WANT A CLOSED LOOP...
44533  0020 00 0 44535       TRA *+2         UP- NO  -GO ON.
44534  0020 00 0 44524       TRA SIB10+4     DN- YES -REP SAME VALUE.
44535  0074 00 4 00104       TSX ERROR-1,4
44536  0020 00 0 44520       TRA SIB10

44537 -0500 00 0 45135  SIB11 CAL LIES
44540  0767 00 0 00001       ALS 1
44541  2 00001 1 44523       TIX SIB10+3,1,1 STEP TO NEXT COL

44542  0074 00 4 00106       TSX OK,4        CONTINUE TEST.
44543  0020 00 0 44520       TRA SIB10       REPEAT TEST.
```

RIPPLE TEST - ONT

```
44544  464563606060          BCD 1ONT
44545  0074 00 4 45152  SIB12 TSX  CLEAR,4
44546  0774 00 1 00043       AXT 35,1
44547 -0500 00 0 45114       CAL BIT35
44550  0602 00 0 45135       SLW LIES
44551 -0500 00 0 45135       CAL LIES
44552  0044 00 0 00000       PAI             SET RESP SI COL
44553  0446 00 0 45135       ONT LIES        SHOULD TRA

44554  0020 00 0 44556       TRA *+2         ERROR
44555  0020 00 0 44563       TRA SIB13       TRY AGAIN.

44556  0760 00 0 00161       SWT 1           WANT A CLOSED LOOP...
44557  0020 00 0 44561       TRA *+2         UP- NO  -GO ON
44560  0020 00 0 44551       TRA SIB12+4     DN- YES -REP SAME VAL.
44561  0074 00 4 00104       TSX ERROR-1,4
44562  0020 00 0 44545       TRA SIB12

44563 -0500 00 0 45135  SIB13 CAL LIES
44564  0767 00 0 00001       ALS 1
44565  2 00001 1 44550       TIX SIB12+3,1,1 STEP TO NEXT COL..

44566  0074 00 4 00106       TSX OK,4        CONTINUE TEST
44567  0020 00 0 44545       TRA SIB12       REPEAT TEST
```

CHECKING ONT AND OFT WITH VARIOUS BIT PATTERNS

```
44570  464563462663          BCD 10NTOFT
44571  0074 00 4 45152  SIB14 TSX  CLEAR,4
44572  0441 00 0 45115        LDI P01S        OCT  111111111111
44573  0446 00 0 45117        ONT P04S        BIT PATT 100  SHOULDNT SKIP
44574  0020 00 0 44577        TRA *+3
44575  0074 00 4 00104        TSX ERROR-1,4
44576  0020 00 0 44571        TRA SIB14
44577  0444 00 0 45117        OFT P04S        SHOULD SKIP
44600  0020 00 0 44602        TRA *+2         ERROR
44601  0020 00 0 44604        TRA *+3         OK- GO ON
44602  0074 00 4 00104        TSX ERROR-1,4
44603  0020 00 0 44571        TRA SIB14

44604  0446 00 0 45116        ONT P02S        BIT PATT 010  -SHOULDNT SKIP
44605  0020 00 0 44610        TRA *+3         OK- GO ON.
44606  0074 00 4 00104        TSX ERROR-1,4
44607  0020 00 0 44571        TRA SIB14

44610  0444 00 0 45116        OFT P02S        SHOULD SKIP...
44611  0020 00 0 44613        TRA *+2         ERROR
44612  0020 00 0 44615        TRA *+3         OK- GO ON.
44613  0074 00 4 00104        TSX ERROR-1,4
44614  0020 00 0 44571        TRA SIB14

44615  0446 00 0 45115        ONT P01S        SHOULD SKIP..
44616  0020 00 0 44620        TRA *+2         ERROR
44617  0020 00 0 44622        TRA *+3         OK- GO ON.
44620  0074 00 4 00104        TSX ERROR-1,4
44621  0020 00 0 44571        TRA SIB14

44622  0444 00 0 45115        OFT P01S        SHOULDNT SKIP..
44623  0020 00 0 44625        TRA *+2         OK-  GO ON.
44624  0074 00 4 00105        TSX ERROR,4
44625  0074 00 4 00106        TSX OK,4        CONTINUE TEST
44626  0020 00 0 44571        TRA SIB14       REPEAT TEST.
```

RIPPLE TESTS- LFT, RFT

WITH XRA CHECKING
2 LFT
1 RFT

```
44627  432663512663              BCD 1LFTRFT
44630  0074 00 4 45152    SIC1   TSX  CLEAR,4
44631  0774 00 1 00002           AXT 2,1          FOR XEC
44632  0774 00 2 00021           AXT 17,2         COUNT DOWN.
44633 -0500 00 1 45115           CAL BIT17+2,1 XRA  2  000001000000
                                               XRA  1  000000000001
44634  0602 00 0 45135           SLW LIES
44635  0441 00 0 45101           LDI BS135        LOAD SI REG
44636 -0500 00 0 45135           CAL LIES
44637  0041 00 0 00000           IIA              TURN OFF SI COL BEING CHD.
44640  0621 00 1 44661           STA SIC1A+2,1
44641  0625 00 1 44661           STT SIC1A+2,1

44642  0522 00 1 44661           XEC SIC1A+2,1 EITHER LFT OR RFT

44643  0020 00 0 44645           TRA *+2          ERROR-SHOULD HAVE SKIPPED.
44644  0020 00 0 44652           TRA SIC1B        OK- TRY AGAIN.

44645  0760 00 0 00161           SWT 1            WANT A CLOSED LOOP...
44646  0020 00 0 44650           TRA *+2          UP-  NO  -GO ON.
44647  0020 00 0 44635           TRA SIC1+5       DN- YES  -REP SAME VAL.

44650  0074 00 4 00104           TSX ERROR-1,4
44651  0020 00 0 44630           TRA SIC1

44652 -0500 00 0 45135    SIC1B  CAL LIES
44653  0767 00 0 00001           ALS 1
44654  2 00001 2 44634           TIX SIC1+4,2,1 STEP TO NEXT COL.
44655  2 00001 1 44632           TIX SIC1+2,1,1 REP FOR RFT.
44656  0020 00 0 44661           TRA *+3

44657 -0054 00  000000    SIC1A  LFT **           TWO INST
44660  0054 00  000000           RFT **             BEING EXECUTED.

44661  0074 00 4 00106           TSX OK,4         CONTINUE TEST.
44662  0020 00 0 44630           TRA SIC1         REPEAT TEST.
```

SECTION THREE

RIPPLE TESTS- LNT, RNT

WITH XRA CHECKING
2 LNT
1 RNT

```
44663  434563514563          BCD 1LNTRNT
44664  0074 00 4 45152  SIC2  TSX  CLEAR,4
44665  0774 00 1 00002        AXT 2,1          FOR XEC
44666  0774 00 2 00021        AXT 17,2         COUNT DOWN.
44667 -0500 00 1 45115        CAL BIT17+2,1    XRA  2  000001000000
                                               XRA  1  000000000001
44670  0602 00 0 45135        SLW LIES
44671 -0500 00 0 45135        CAL LIES
44672  0044 00 0 00000        PAI              TURN ON RESP SI COL
44673  0621 00 1 44714        STA SIC2A+2,1
44674  0625 00 1 44714        STT SIC2A+2,1

44675  0522 00 1 44714        XEC SIC2A+2,1    EITHER LNT OR RNT.

44676  0020 00 0 44700        TRA *+2          ERROR-SHOULDVE SKIPPED.
44677  0020 00 0 44705        TRA SIC2B        OK- TRY AGAIN.

44700  0760 00 0 00161        SWT 1            WANT A CLOSED LOOP...
44701  0020 00 0 44703        TRA *+2          UP-  NO  -GO ON.
44702  0020 00 0 44671        TRA SIC2+5       DN- YES  -REP SAME VAL.

44703  0074 00 4 00104        TSX ERROR-1,4
44704  0020 00 0 44664        TRA SIC2

44705 -0500 00 0 45135  SIC2B CAL LIES
44706  0767 00 0 00001        ALS 1
44707  2 00001 2 44670        TIX SIC2+4,2,1   STEP TO NEXT COL

44710  2 00001 1 44666        TIX SIC2+2,1,1   REP FOR RNT
44711  0020 00 0 44714        TRA *+3


44712 -0056 00  000000  SIC2A LNT **
44713  0056 00  000000        RNT **


44714  0074 00 4 00106        TSX OK,4         CONTINUE TEST.
44715  0020 00 0 44664        TRA SIC2         REPEAT TEST.
```

CHECKING RFT WITH VARIOUS BIT PATTERNS

```
44716  512663606060              BCD 1RFT
44717  0074 00 4 45152    SIC3   TSX  CLEAR,4
44720  0441 00 0 45115           LDI P01S        OCT  111111111111
44721  0054 00  444444           RFT 444444      SHOULD SKIP-
44722  0020 00 0 44724           TRA *+2         ERROR-
44723  0020 00 0 44726           TRA *+3         OK-GO ON.
44724  0074 00 4 00104           TSX ERROR-1,4
44725  0020 00 0 44717           TRA SIC3

44726  0054 00  222222           RFT 222222      SHOULD SKIP-
44727  0020 00 0 44731           TRA *+2         ERROR-
44730  0020 00 0 44733           TRA *+3         OK-GO ON.
44731  0074 00 4 00104           TSX ERROR-1,4
44732  0020 00 0 44717           TRA SIC3

44733  0054 00  111111           RFT 111111      SHOULDNT SKIP
44734  0020 00 0 44736           TRA *+2         OK-  GO ON.
44735  0074 00 4 00105           TSX ERROR,4
44736  0074 00 4 00106           TSX OK,4        CONTINUE TEST
44737  0020 00 0 44717           TRA SIC3        REPEAT TEST
```

CHECKING LFT WITH VARIOUS BIT PATTERNS

```
44740  432663606060              BCD 1LFT
44741  0074 00 4 45152    SIC4   TSX  CLEAR,4
44742  0441 00 0 45115           LDI P01S        OCT  111111111111
44743 -0054 00  444444           LFT 444444      SHOULD SKIP..
44744  0020 00 0 44746           TRA *+2         ERROR-
44745  0020 00 0 44750           TRA *+3         OK- GO ON.
44746  0074 00 4 00104           TSX ERROR-1,4
44747  0020 00 0 44741           TRA SIC4

44750 -0054 00  222222           LFT 222222      SHOULD SKIP..
44751  0020 00 0 44753           TRA *+2         ERROR-
44752  0020 00 0 44755           TRA *+3         OK- GO ON.
44753  0074 00 4 00104           TSX ERROR-1,4
44754  0020 00 0 44741           TRA SIC4

44755 -0054 00  111111           LFT 111111      SHOULDNT SKIP..
44756  0020 00 0 44760           TRA *+2         OK- GO ON.
44757  0074 00 4 00105           TSX ERROR,4
44760  0074 00 4 00106           TSX OK,4        CONTINUE TEST
44761  0020 00 0 44741           TRA SIC4        REPEAT TEST
```

CHECKING RNT WITH VARIOUS BIT PATTERNS

```
44762  514563606060              BCD 1RNT
44763  0074 00 4 45152   SIC5    TSX  CLEAR,4
44764  0441 00 0 45115           LDI POIS        OCT  111111111111
44765  0056 00  444444           RNT 444444      SHOULDNT SKIP..
44766  0020 00 0 44771           TRA *+3         OK- GO ON.
44767  0074 00 4 00104           TSX ERROR-1,4 ERROR-
44770  0020 00 0 44763           TRA SIC5

44771  0056 00  222222           RNT 222222      SHOULDNT SKIP..
44772  0020 00 0 44775           TRA *+3         OK- GO ON.
44773  0074 00 4 00104           TSX ERROR-1,4 ERROR
44774  0020 00 0 44763           TRA SIC5

44775  0056 00  111111           RNT 111111      SHOULD SKIP..
44776  0020 00 0 45000           TRA *+2         ERROR
44777  0020 00 0 45001           TRA *+2         OK- GO ON.
45000  0074 00 4 00105           TSX ERROR,4
45001  0074 00 4 00106           TSX OK,4        CONTINUE TEST
45002  0020 00 0 44763           TRA SIC5        REPEAT TEST
```

CHECKING LNT WITH VARIOUS BIT PATTERNS

```
45003  434563606060              BCD 1LNT
45004  0074 00 4 45152   SIC6    TSX  CLEAR,4
45005  0441 00 0 45115           LDI POIS        OCT  111111111111
45006 -0056 00  444444           LNT 444444      SHOULDNT SKIP..
45007  0020 00 0 45012           TRA *+3         OK- GO ON.
45010  0074 00 4 00104           TSX ERROR-1,4
45011  0020 00 0 45004           TRA SIC6

45012 -0056 00  222222           LNT 222222      SHOULDNT SKIP..
45013  0020 00 0 45016           TRA *+3         OK- GO ON.
45014  0074 00 4 00104           TSX ERROR-1,4
45015  0020 00 0 45004           TRA SIC6

45016 -0056 00  111111           LNT 111111      SHOULD SKIP..
45017  0020 00 0 45021           TRA *+2         ERROR
45020  0020 00 0 45022           TRA *+2         OK- GO ON.
45021  0074 00 4 00105           TSX ERROR,4
45022  0074 00 4 00106           TSX OK,4        CONTINUE TEST
45023  0020 00 0 45004           TRA SIC6        REPEAT TEST
```

TESTING SI INST USING INDIRECT ADDRESSING

```
45024   623151437060            BCD 1SIRLY
45025   0074 00 4 45152   SID0  TSX  CLEAR,4
45026   0441 00 0 45101         LDI BS135
45027   0440 60  045030         IIS* *+1
45030   0761 00 0 45101         NOP BS135
45031  -0046 00 0 00000         PIA
45032   0100 00 0 45034         TZE *+2
45033   0074 00 4 00105         TSX ERROR,4
45034   0074 00 4 00106         TSX OK,4        CONTINUE TEST.
45035   0020 00 0 45025         TRA SID0        REPEAT TEST.

45036   623151437060            BCD 1SIRLY
45037   0074 00 4 45152   SID1  TSX  CLEAR,4
45040   0774 00 1 00001         AXT 1,1
45041   0774 00 2 77776         AXT -2,2
                                                CORR COND OF SI REG
45042  -0500 00 0 45115         CAL P01S        OCT 111111111111
45043   0441 00 2 45077         LDI BS135-2,2               777777777777
45044  -0042 00 0 00000         RIA                          666666666666
45045   0445 00 1 45117         RIS P02S+1,1                 444444444444
45046   0445 00 2 45114         RIS P02S-2,2                 444444444444
45047   0440 00  145120         IIS P04S+1,1                 000000000000
45050   0442 00 1 45117         OSI P02S+1,1                 222222222222
45051   0442 00 2 45115         OSI P04S-2,2                 666666666666
45052   0046 00 0 45054         TIF *+2
45053   0074 00 4 00105         TSX ERROR,4
45054   0074 00 4 00106         TSX OK,4        CONTINUE TEST.
45055   0020 00 0 45037         TRA SID1        REPEAT TEST.


45056   623151437060            BCD 1SIRLY
45057   0074 00 4 45152   SID2  TSX  CLEAR,4
45060   0774 00 1 00001         AXT 1,1
45061   0761 00 0 45101         NOP BS135
45062  -0500 00 0 45115         CAL P01S
45063   0761 00 0 45100         NOP BZERO
                                                CORR COND OF SI REG
45064   0442 60 0 45061         OSI* SID2+2     OSI BS135    777777777777
45065   0445 60 0 45071         RIS* SID2A      RIS P01S     666666666666
45066   0440 60  145062         IIS* SID2+3,1   IIS BS135    111111111111
45067   0042 60 1 45073         TIO* SID2A+2,1

45070   0020 00 0 45073         TRA *+3         ERROR.

45071   0761 00 1 45116   SID2A NOP  P01S+1,1
45072   0761 00 0 45074         NOP *+2
45073   0074 00 4 00105         TSX ERROR,4
45074   0074 00 4 00106         TSX OK,4        CONTINUE TEST.
45075   0020 00 0 45057         TRA SID2        REPEAT TEST.

45076   0 00000 0 00003         PZE  3
45077   0074 00 4 00111         TSX  LOOP,4
```

SECTION THREE
CONSTANTS

```
45100 +000000000000        BZERO OCT +0
45101 -377777777777        BS135 OCT -377777777777
45102 +000000777777        SIRH1 OCT +000000777777
45103 -377777000000        SILH1 OCT -377777000000
45104 +050505050505        P05S  OCT 050505050505
45105 +070707070707        P07S  OCT 070707070707
45106 -377777000001        P1835 OCT 777777000001
45107 +252525252525        P25S  OCT +252525252525
45110 -125252525252        P52S  OCT -125252525252
45111 -155555555555        P55S  OCT 555555555555
45112 +100000000000        BIT1  OCT 100000000000
45113 +000001000000        BIT17 OCT 000001000000
45114 +000000000001        BIT35 OCT +1

45115 +111111111111        P01S  OCT 111111111111
45116 +222222222222        P02S  OCT 222222222222
45117 -044444444444        P04S  OCT 444444444444
45120 +333333333333        P03S  OCT 333333333333
45121 -365432112345        SIBP1 OCT 765432112345

45122 -1 00000 0 00000     INTL1 STR                 INSTRUCTIONS TO BE
45123  0021 00 0 45203           TTR TRAPS+1          PUT IN LOCATIONS
45124 +000000000200        P002  OCT 200             PRIMARY OP 02
45125 +000000000040        TR    OCT 40              TO INDICATE TRAP TGR ON.

45126  0441 00 0 45101     LOAD  LDI BS135
45127  0442 00 0 45101           OSI BS135
45130  0044 00 0 00000           PAI
45131  0043 00 0 00000           OAI
45132  0041 00 0 00000           IIA
45133  0440 00  045101           IIS BS135
45134 +000000000000              OCT +0

                    45135  LIES  BSS 7              TEMP FOR TEST ROUTINES.

                    45144  SHOPS BSS 6              TEMP FOR SUBROUTINES.
```

PROGRAM RESET SUBROUTINE.

SUBROUTINE USED TO CLEAR ALL MF REGISTERS.

```
45152  1 77777 4 45153   CLEAR TXI  *+1,4,-1
45153  0636 00 4 45201         SCA  RETN,4
45154  0761 00 0 00000         NOP
45155  0500 00 0 45122         CLA INTL1      L-100000000000 STR INST.
45156  0601 00 0 00000         STO            RESET ZERO - POST RESTART.
45157 -0754 00 0 00000         PXD            CLEARING MQ
45160  0131 00 0 00000         XCA                    AND
45161 -0754 00 0 00000         PXD                       ACC.
45162  0140 00 0 45163         TOV *+1        TURN OFF ACC OV TGR.
45163  0760 00 0 00144         SLN  4
45164  0044 00 0 00000         PAI
          SI INST USED IN CLEARING SI REG. IF PAI DOES NOT
          END OPERATION, IT WILL HANG-UP IN THIS ROUTINE.

45165  0774 00 1 00007         AXT 7,1        CLEARING
45166  0600 00 1 45144         STZ LIES+7,1           PROGRAM
45167  2 00001 1 45166         TIX *-1,1,1                   TEMP LOC.
45170  0760 00 0 00016         LMTM
45171  0774 00 7 00000         AXT 0,7        CLEAR XRA, XRB, XRC.
45172  0774 00 6 00000         AXT  0,6          XRD,XRE,XRF
45173  0774 00 5 00000         AXT  0,5
45174  0774 00 4 00000         AXT  0,4
45175  0774 00 3 00000         AXT  0,3
45176  0774 00 2 00000         AXT  0,2
45177  0774 00 1 00000         AXT  0,1
45200 -0760 00 0 00016         EMTM

45201  0020 00 0 00000   RETN  TRA **          RET TO TEST LOCATION.
```

PROGRAM TRAP CONTROL

SUBROUTINE USED TO CHECK ALL TEST ROUTINE OPERATIONS THAT CAUSE THE PROGRAM TO TRAP TO LOCATION 00001.

IF A LEGAL TRAP, THE TEST ROUTINE WILL FURNISH AN ADDRESS SO THAT CONTROL WILL BE RETURNED TO TEST LOCATION.

```
45202  0000 00 0 00000   TRAPS HTR **          TEST ROUT SUPPL ADDR.
45203 -0760 00 0 00007         LTM            JUST IN CASE.
45204 -0520 00 0 45202         NZT TRAPS      WAS AN ADDR SUPPLIED...
45205  0020 00 0 45213         TRA TRPS1      NO- WHAT GIVES HERE...
45206  0534 00 4 45202         LXA TRAPS,4          - OK.  GET RETURN.
45207  0600 00 0 45202         STZ TRAPS      RESET BEFORE NEXT TRAP.
45210  0634 00 4 45212         SXA *+2,4
45211  0774 00 4 00000         AXT 0,4        CLEAR XRC.
45212  0020 00 0 00000         TRA **         RETURN TO TEST ROUTINE.
```

```
  NO ADDRESS WAS SUPPLIED BY MAIN PROGRAM.  CHECK IS NOW MADE
 TO SEE IF PROGRAM TRAPPED TO LOCATION 00001 IN ERROR
 OR SKIPPED TO LOCATION 00001 IN ERROR.

45213  0634 00 1 45152   TRPS1 SXA SHOPS+6,1  STORE XRA
45214  0534 00 1 00000         LXA 0,1        ADDRESS OF LOC 00000.
45215  3 00000 1 45221         TXH TRPS2,1,0 DID WE STORE ADDR AT 00000.
45216 -0774 00 4 00001         AXC 1,4        NO- TRA TO SEQ ER
45217  0534 00 1 45152         LXA SHOPS+6,1 RESTORE XRA.
45220  0020 00 0 00103         TRA SEQER          FOR INDICATION OF ERROR

                    PROGRAM SKIPPED TO LOCATION 00001 IN ERROR.
                    TRANSFER TO SEQER ROUT TO PRINT ERROR.

                    PROGRAM TRAPPED TO LOCATION 00001 IN ERROR.

45221  0634 00 1 45151   TRPS2 SXA SHOPS+5,1 SAVE FOR PRINTOUT.
45222  1 00001 1 45223         TXI *+1,1,1   STEP ONE FOR RETURN.
45223  0634 00 1 45232         SXA SWTWO,1   TO TRANSFER BACK
45224  0634 00 1 45235         SXA SWTHR,1      TO TEST ROUTINE.
45225  0634 00 1 45254         SXA  LST,1
45226  0560 00 0 45151         LDQ  SHOPS+5
45227  0534 00 1 45152         LXA SHOPS+6,1 RESTORE XRA.

45230  0760 00 0 00162         SWT 2         WANT TO BYPASS ERROR...
45231  0020 00 0 45233         TRA *+2       UP- NO.
45232  0020 00 0 00000   SWTWO TRA **        DN- YES.
45233  0760 00 0 00163         SWT  3
45234  0020 00 0 45236         TRA  *+2        UP - PRINT
45235  0000 00 0 00000   SWTHR HTR **        DN- HALT ON ERROR.

        ACC 21-35 CONTAINS TRAP LOC ADDR.

45236  0767 00 0 00022         ALS  18
45237  0074 00 4 74302         TSX  PX,4
45240 -0600 00 0 45253         STQ  LST-1
45241  0074 00 4 74300         TSX  SPLAT,4
45242  0 00014 0 00011         PZE  9,0,12
45243  475146275121            BCD 6PROGRAM TRAPPED TO LOCATION 00001 IN
45244  446063512147
45245  472524606346
45246  604346232163
45247  314645600000
45250  000001603145
45251  602551514651            BCD 3 ERROR FROM
45252  602651464460
45253  606060606060
45254  0020 00 0 00000  LST    TRA  **
```