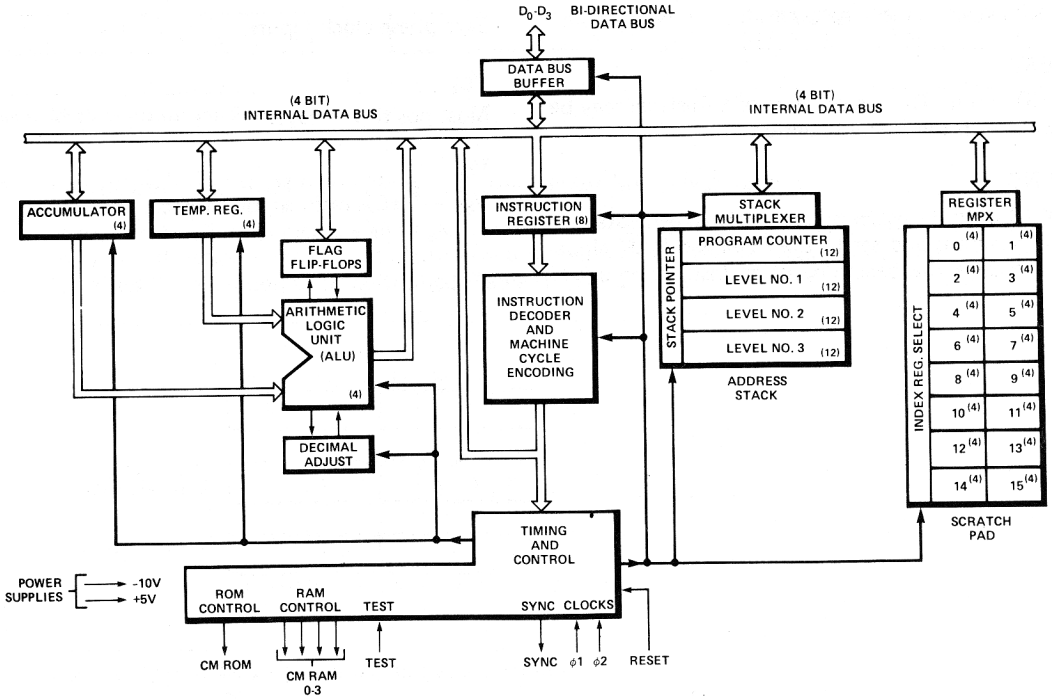
4004
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- 4-Bit Parallel CPU With 46 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes
- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-40 ROMs and RAMs
- Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- Standard Operating Temperature Range of 0° to 70°C
- Also Available With -40° to +85°C Operating Range

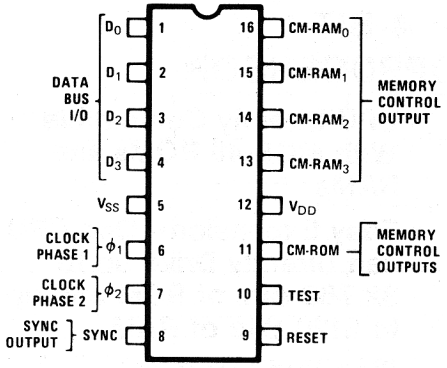
The Intel® 4004 is a complete 4-bit parallel central processing unit (CPU). The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.



Pin Description



D_0-D_3

BIDIRECTIONAL DATA BUS. All address and data communication between the processor and the RAM and ROM chips occurs on these 4 lines.

RESET

RESET input. A logic "1" level at this input clears all flags and status registers and forces the program counter to zero. To completely clear all address and index registers, RESET must be applied for 64 clock cycles (8 machine cycles).

TEST

TEST input. The logical state of this signal may be tested with the JCN instruction.

SYNC

SYNC output. Synchronization signal generated by the processor and set to the ROM and RAM chips. It indicates the beginning of an instruction cycle.

CM-ROM

CM-ROM output. This is the ROM selection signal sent out by the processor when data is required from program memory.

CM-RAM$_0$ – CM-RAM$_3$

CM-RAM outputs. These are the bank selection signals for the 4002 RAM chips in the system.

ϕ_1, ϕ_2

Two phase clock inputs.

V_{SS}

Most positive voltage.

V_{DD}

V_{SS} -15 ±5% main supply voltage.

Instruction Set Format

A. Machine Instructions

- 1 word instruction – 8-bits requiring 8 clock periods (instruction cycle).
- 2 word instruction – 16-bits requiring 16 clock periods (2 instruction cycles).

Each instruction is divided into two four-bit fields. The upper 4-bits is the OPR field containing the operation code. The lower 4-bits is the OPA field containing the modifier. For two word instructions, the second word contains address information or data.

The upper 4-bits (OPR) will always be fetched before the lower 4-bits (OPA) during M_1 and M_2 times respectively.

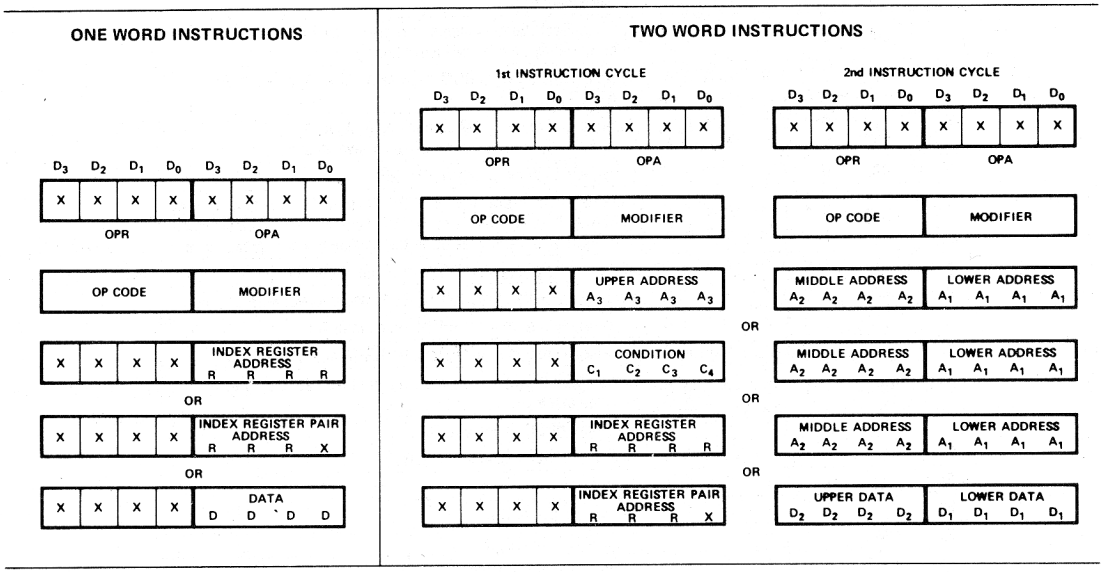


Table I. Machine Instruction Format

B. Input/Output and RAM Instructions and Accumulator Group Instructions

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed. Table II illustrates the contents of each 4-bit field.

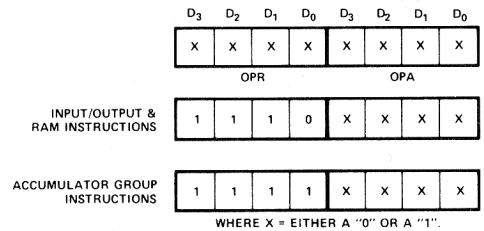


Table II. I/O and Accumulator Group Instruction Formats

4004 Instruction Set

BASIC INSTRUCTIONS (* = 2 Word Instructions)

Hex Code	MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
00	NOP	0 0 0 0	0 0 0 0	No operation.
1 - -	*JCN	0 0 0 1 $A_2 A_2 A_2 A_2$	$C_1 C_2 C_3 C_4$ $A_1 A_1 A_1 A_1$	Jump to ROM address $A_2 A_2 A_2 A_2$, $A_1 A_1 A_1 A_1$ (within the same ROM that contains this JCN instruction) if condition $C_1 C_2 C_3 C_4$ is true, otherwise go to the next instruction in sequence.
2 - -	*FIM	0 0 1 0 $D_2 D_2 D_2 D_2$	R R R 0 $D_1 D_1 D_1 D_1$	Fetch immediate (direct) from ROM Data $D_2 D_2 D_2 D_2 D_1 D_1 D_1 D_1$ to index register pair location RRR.
3 -	FIN	0 0 1 1	R R R 0	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.
3 -	JIN	0 0 1 1	R R R 1	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the instruction cycle.
4 - -	*JUN	0 1 0 0 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump unconditional to ROM address $A_3 A_3 A_3 A_3 A_2 A_2 A_2 A_2$ $A_1 A_1 A_1 A_1$.
5 - -	*JMS	0 1 0 1 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump to subroutine ROM address $A_3 A_3 A_3 A_3 A_2 A_2 A_2 A_2$ $A_1 A_1 A_1 A_1$, save old address (up 1 level in stack.)
6 -	INC	0 1 1 0	R R R R	Increment contents of register RRRR.
7 - -	*ISZ	0 1 1 1 $A_2 A_2 A_2 A_2$	R R R R $A_1 A_1 A_1 A_1$	Increment contents of register RRRR. Go to ROM address $A_2 A_2 A_2$ $A_1 A_1 A_1 A_1$ (within the same ROM that contains this ISZ instruction) if result $\neq 0$, otherwise go to the next instruction in sequence.
8 -	ADD	1 0 0 0	R R R R	Add contents of register RRRR to accumulator with carry.
9 -	SUB	1 0 0 1	R R R R	Subtract contents of register RRRR to accumulator with borrow.
A -	LD	1 0 1 0	R R R R	Load contents of register RRRR to accumulator.
B -	XCH	1 0 1 1	R R R R	Exchange contents of index register RRRR and accumulator.
C -	BBL	1 1 0 0	D D D D	Branch back (down 1 level in stack) and load data DDDD to accumulator.
D -	LDM	1 1 0 1	D D D D	Load data DDDD to accumulator.
F0	CLB	1 1 1 1	0 0 0 0	Clear both. (Accumulator and carry)
F1	CLC	1 1 1 1	0 0 0 1	Clear carry.
F2	IAC	1 1 1 1	0 0 1 0	Increment accumulator.
F3	CMC	1 1 1 1	0 0 1 1	Complement carry.
F4	CMA	1 1 1 1	0 1 0 0	Complement accumulator.
F5	RAL	1 1 1 1	0 1 0 1	Rotate left. (Accumulator and carry)
F6	RAR	1 1 1 1	0 1 1 0	Rotate right. (Accumulator and carry)
F7	TCC	1 1 1 1	0 1 1 1	Transmit carry to accumulator and clear carry.
F8	DAC	1 1 1 1	1 0 0 0	Decrement accumulator.
F9	TCS	1 1 1 1	1 0 0 1	Transfer carry subtract and clear carry.
FA	STC	1 1 1 1	1 0 1 0	Set carry.
FB	DAA	1 1 1 1	1 0 1 1	Decimal adjust accumulator.
FC	KBP	1 1 1 1	1 1 0 0	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
FD	DCL	1 1 1 1	1 1 0 1	Designate command line.

4001/4002/4008/4009/4289 INPUT/OUTPUT AND RAM INSTRUCTIONS

Hex Code	MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
2 -	SRC	0 0 1 0	R R R 1	Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the instruction cycle.
E0	WRM	1 1 1 0	0 0 0 0	Write the contents of the accumulator into the previously selected RAM main memory character.
E1	WMP	1 1 1 0	0 0 0 1	Write the contents of the accumulator into the previously selected RAM output port. (Output Lines)
E2	WRR	1 1 1 0	0 0 1 0	Write the contents of the accumulator into the previously selected ROM output port. (I/0 Lines)
E3	WPM	1 1 1 0	0 0 1 1	Write the contents of the accumulator into the previously selected half byte of read/write program memory (used with 4008/4009 or 4289 only)
E4	WR0	1 1 1 0	0 1 0 0	Write the contents of the accumulator into the previously selected RAM status character 0.
E5	WR1	1 1 1 0	0 1 0 1	Write the contents of the accumulator into the previously selected RAM status character 1.
E6	WR2	1 1 1 0	0 1 1 0	Write the contents of the accumulator into the previously selected RAM status character 2.
E7	WR3	1 1 1 0	0 1 1 1	Write the contents of the accumulator into the previously selected RAM status character 3.
E8	SBM	1 1 1 0	1 0 0 0	Subtract the previously selected RAM main memory character from accumulator with borrow.
E9	RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator.
EA	RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator. (I/0 Lines)
EB	ADM	1 1 1 0	1 0 1 1	Add the previously selected RAM main memory character to accumulator with carry.
EC	RD0	1 1 1 0	1 1 0 0	Read the previously selected RAM status character 0 into accumulator.
ED	RD1	1 1 1 0	1 1 0 1	Read the previously selected RAM status character 1 into accumulator.
EE	RD2	1 1 1 0	1 1 1 0	Read the previously selected RAM status character 2 into accumulator.
EF	RD3	1 1 1 0	1 1 1 1	Read the previously selected RAM status character 3 into accumulator.

4004 Instruction Codes

Hex	Mnemonic		Hex	Mnemonic		Hex	Mnemonic		Hex	Mnemonic	
00	–		40	JUN		80	ADD	0	C0	BBL	0
01	–		41	JUN		81	ADD	1	C1	BBL	1
02	–		42	JUN		82	ADD	2	C2	BBL	2
03	–		43	JUN		83	ADD	3	C3	BBL	3
04	–		44	JUN		84	ADD	4	C4	BBL	4
05	–		45	JUN		85	ADD	5	C5	BBL	5
06	–		46	JUN		86	ADD	6	C6	BBL	6
07	–		47	JUN		87	ADD	7	C7	BBL	7
08	–		48	JUN		88	ADD	8	C8	BBL	8
09	–		49	JUN		89	ADD	9	C9	BBL	9
0A	–		4A	JUN		8A	ADD	10	CA	BBL	10
0B	–		4B	JUN		8B	ADD	11	CB	BBL	11
0C	–		4C	JUN		8C	ADD	12	CC	BBL	12
0D	–		4D	JUN		8D	ADD	13	CD	BBL	13
0E	–		4E	JUN	Second hex	8E	ADD	14	CE	BBL	14
0F	–		4F	JUN	digit is part	8F	ADD	15	CF	BBL	15
10	JCN	CN=0	50	JMS	of jump	90	SUB	0	D0	LDM	0
11	JCN	CN=1 also JNT	51	JMS	address.	91	SUB	1	D1	LDM	1
12	JCN	CN=2 also JC	52	JMS		92	SUB	2	D2	LDM	2
13	JCN	CN=3	53	JMS		93	SUB	3	D3	LDM	3
14	JCN	CN=4 also JZ	54	JMS		94	SUB	4	D4	LDM	4
15	JCN	CN=5	55	JMS		95	SUB	5	D5	LDM	5
16	JCN	CN=6	56	JMS		96	SUB	6	D6	LDM	6
17	JCN	CN=7	57	JMS		97	SUB	7	D7	LDM	7
18	JCN	CN=8	58	JMS		98	SUB	8	D8	LDM	8
19	JCN	CN=9 also JT	59	JMS		99	SUB	9	D9	LDM	9
1A	JCN	CN=10 also JNC	5A	JMS		9A	SUB	10	DA	LDM	10
1B	JCN	CN=11	5B	JMS		9B	SUB	11	DB	LDM	11
1C	JCN	CN=12 also JNZ	5C	JMS		9C	SUB	12	DC	LDM	12
1D	JCN	CN=13	5D	JMS		9D	SUB	13	DD	LDM	13
1E	JCN	CN=14	5E	JMS		9E	SUB	14	DE	LDM	14
1F	JCN	CN=15	5F	JMS		9F	SUB	15	DF	LDM	15
20	FIM	0	60	INC	0	A0	LD	0	E0	WRM	
21	SRC	0	61	INC	1	A1	LD	1	E1	WMP	
22	FIM	2	62	INC	2	A2	LD	2	E2	WRR	
23	SRC	2	63	INC	3	A3	LD	3	E3	WPM	
24	FIM	4	64	INC	4	A4	LD	4	E4	WR0	
25	SRC	4	65	INC	5	A5	LD	5	E5	WR1	
26	FIM	6	66	INC	6	A6	LD	6	E6	WR2	
27	SRC	6	67	INC	7	A7	LD	7	E7	WR3	
28	FIM	8	68	INC	8	A8	LD	8	E8	SBM	
29	SRC	8	69	INC	9	A9	LD	9	E9	RDM	
2A	FIM	10	6A	INC	10	AA	LD	10	EA	RDR	
2B	SRC	10	6B	INC	11	AB	LD	11	EB	ADM	
2C	FIM	12	6C	INC	12	AC	LD	12	EC	RD0	
2D	SRC	12	6D	INC	13	AD	LD	13	ED	RD1	
2E	FIM	14	6E	INC	14	AE	LD	14	EE	RD2	
2F	SRC	14	6F	INC	15	AF	LD	15	EF	RD3	
30	FIN	0	70	ISZ	0	B0	XCH	0	F0	CLB	
31	JIN	0	71	ISZ	1	B1	XCH	1	F1	CLC	
32	FIN	2	72	ISZ	2	B2	XCH	2	F2	IAC	
33	JIN	2	73	ISZ	3	B3	XCH	3	F3	CMC	
34	FIN	4	74	ISZ	4	B4	XCH	4	F4	CMA	
35	JIN	4	75	ISZ	5	B5	XCH	5	F5	RAL	
36	FIN	6	76	ISZ	6	B6	XCH	6	F6	RAR	
37	JIN	6	77	ISZ	7	B7	XCH	7	F7	TCC	
38	FIN	8	78	ISZ	8	B8	XCH	8	F8	DAC	
39	JIN	8	79	ISZ	9	B9	XCH	9	F9	TCS	
3A	FIN	10	7A	ISZ	10	BA	XCH	10	FA	STC	
3B	JIN	10	7B	ISZ	11	BB	XCH	11	FB	DAA	
3C	FIN	12	7C	ISZ	12	BC	XCH	12	FC	KBP	
3D	JIN	12	7D	ISZ	13	BD	XCH	13	FD	DCL	
3E	FIN	14	7E	ISZ	14	BE	XCH	14	FE	–	
3F	JIN	14	7F	ISZ	15	BF	XCH	15	FF	–	

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to V_{SS} ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

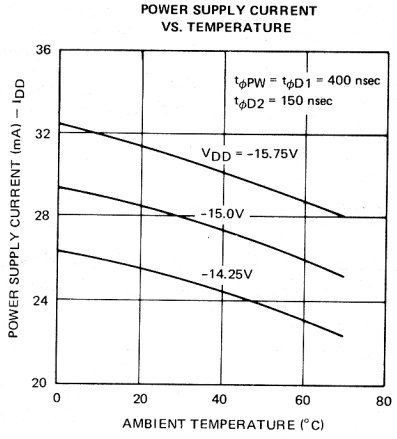
D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ± 5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		30	40	mA	T_A=25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL}=V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	4004 TEST Input
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT}=-12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitance Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT}=V_{SS}
I_{OL}	CM-ROM Sinking Current	6.5	12		mA	V_{OUT}=V_{SS}
I_{OL}	CM-RAM Sinking Current	2.5	6		mA	V_{OUT}=V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL}=0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-ROM Output Resistance, Data Line "0" Level		320	600	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-RAM Output Resistance, Data Line "0" Level		1.1	1.8	kΩ	V_{OUT}=V_{SS}-.5V
CAPACITANCE						
C_{ϕ}	Clock Capacitance		14	20	pF	V_{IN}=V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN}=V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN}=V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN}=V_{SS}

Typical D.C. Characteristics



A.C. Characteristics

T_A=0°C to 70°C, V_{SS}-V_{DD} = 15V ±5%

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t_{\phi R}$	Clock Rise Time			50	ns	
$t_{\phi F}$	Clock Fall Times			50	ns	
$t_{\phi PW}$	Clock Width	380		480	ns	
$t_{\phi D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t_{\phi D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_H[3]	Data Bus Hold Time During M_2-X_1 and and X_2-X_3 Transition.	150			ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	Data Lines			700	ns	200pF Data Lines[4]
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT}=20pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to the 4004 at M_2 and X_2 always enter a float state until the 4004 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. $C_{DATA\ BUS}$ = 200pF if 4008 and 4009 or 4289 is used.

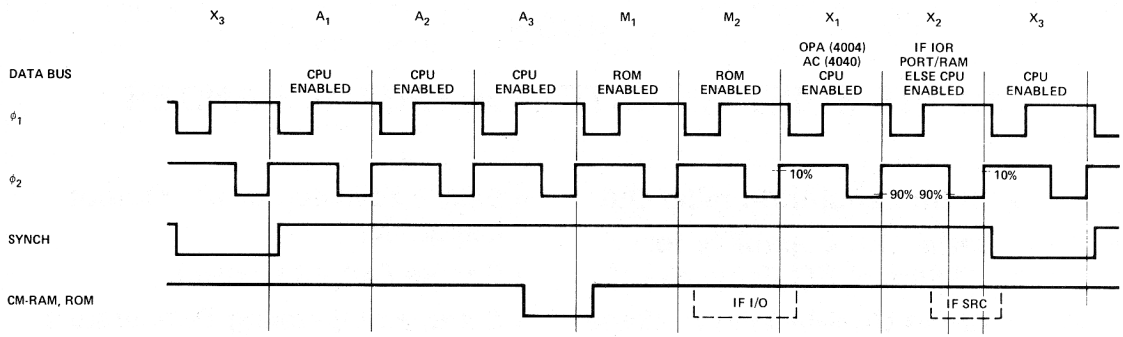


Figure 1. Timing Diagram.

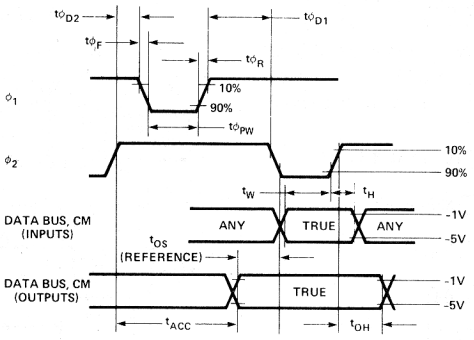


Figure 2. Timing Detail.

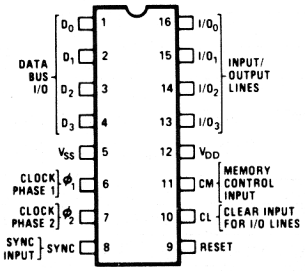
4001

256 x 8 MASK PROGRAMMABLE ROM AND 4 BIT I/O PORT

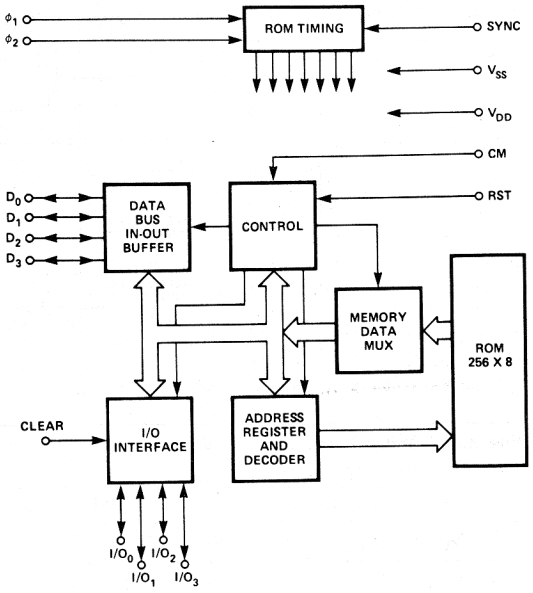
- **Direct Interface to MCS-40™ 4 Bit Data Bus**
- **I/O Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4001 performs two basic and distinct functions. As a ROM it stores 256 x 8 words of program or data tables; as a vehicle of communication with peripheral devices it is provided with 4 I/O pins and associated control logic to perform input and output operations. The 4001 is a PMOS device, compatible with all other MCS-40™ devices.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0 -D_3/Neg.	Bidirectional data bus. All address and data communication between the processor and ROM is handled by these lines.
5	V_{SS}	Most positive supply voltage.
6-7	$\phi1$, $\phi2$/Neg.	Non-overlapped clock signals which determine device timing.
8	SYNC/Neg.	System synchronization signal generated by processor.
9	RESET/Neg.	Reset input. A negative level (V_{DD}) on this pin will clear internal flip-flops and buffers. The input buffers are not cleared by this signal.
10	CL/Neg.	Clear input for I/O lines. A negative level on this pin will clear the I/O buffers. This pin may be driven by a TTL output and a 1K pull-up to V_{SS}.
11	CM-ROM/Neg.	Chip enable generated by the processor.
12	V_{DD}	Main supply voltage value. Must be V_{SS} – 15.0V ±5%.
13-16	I/O_0-I/O_3/Neg.	A single I/O port consisting of 4 bidirectional and selectable lines.

Functional Description

Address and data are transferred in and out by time multiplexing on 4 data bus lines. Timing is internally generated using two clock signals, ϕ_1 and ϕ_2, and a SYNC signal supplied by the CPU. Addresses are received from the CPU on three time periods following SYNC, and select 1 out of 256 words and 1 out of 16 ROM's. For that purpose, each ROM is identified as #0, 1, 2, through 15, by metal option. A Command ROM Line (CM-ROM) is also provided and it is used to select a ROM bank (group of 16 ROM's).

During the two time periods of the instruction cycle (M_1 & M_2) following the addressing time, information is transferred from the ROM to the data bus lines.

A second mode of operation of the ROM is as an Input/Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O external lines. Each chip has the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction. An external signal (CL) will asynchronously clear the output register during normal operation.

All internal flip flops (including the output register) will be reset when the RESET line goes low (V_{DD}).

I/O Options

Each I/O pin on each ROM can be uniquely chosen to be either an input or output line by metal option. Also each input or output can either be inverted or direct. When the pin is chosen as an input it may have an on-chip resistor connected to either V_{DD} or V_{SS}.

Instruction Execution

The 4001 responds to the following instructions.

1. **SRC Instruction** (Send address to ROM and RAM)

   When the CPU executes an SRC instruction it will send out 8 bits of data during X_2 and X_3 and will activate the CM-ROM and one CM-RAM line at X_2. Data at X_2, (representing the contents of the first register of the register pair addressed by the SRC instruction) with simultaneous presence of CM-ROM, is interpreted by the 4001 as the chip number of the unit that should later perform an I/O operation. Data at X_3 is ignored.

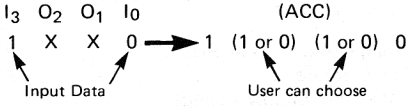
2. **WRR – Write ROM Port**

   The content of the accumulator is transferred to the ROM output port of the previously selected ROM chip. The data is available on the output pins until a new WRR is executed on the same chip. The ACC content and carry/link are unaffected. (The LSB bit of the accumulator appears on I/O_0.) No operation is performed on I/O lines coded as inputs.

3. **RDR – Read ROM Port**

   The data present at the input lines of the previously selected ROM chip is transferred to the accumulator.

   If the I/O option has both inputs and outputs within the same 4 I/O lines, the user can choose to have either "0" or "1" transferred to the accumulator for those I/O pins coded as outputs, when an RDR instruction is executed. For example, given a port with the I/O lines coded with 2 inputs and 2 outputs, when RDR is executed, the transfer is as shown below:



Timing Consideration

In the ROM mode of operation the 4001 will receive an 8 bit address during A_1 and A_2 times of the instruction cycle and a chip number, together with CM-ROM, during A_3 time. When CM-ROM is present, only the chip whose metal option code matches the chip number code sent during A_3 is allowed to send data out during the following two cycles: M_1 and M_2. The activity of the 4001 in the ROM mode ends at M_2.

The 4001 can have a chip number via the metal option from 0 – 15.

In the I/O mode of operation, the selected 4001 (by SRC), after receiving RDR will transfer the information present at its I/O pins to the data bus at X_2. If the instruction received was WRR, the data present on the data bus at $X_2 \cdot \phi_2$ will be latched on the output flip-flops associated with the I/O lines.

Ordering Information

When ordering a 4001, the following information must be specified:

1. Chip number
2. All the metal options for *each* I/O pin.
3. ROM pattern to be stored in each of the 256 locations.

A blank customer truth table is available upon request from Intel. A copy of this table is shown and blank copy can be found following the detailed 4001 characteristics.

EXAMPLES – DESIRED OPTION/CONNECTIONS REQUIRED

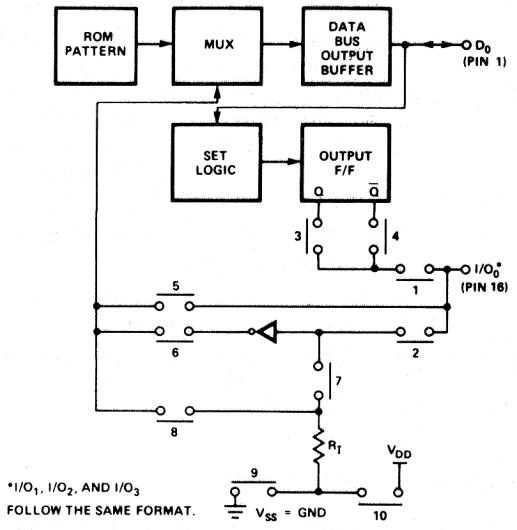
1. Non-inverting output (negative logic output) – 1 and 3 are connected.
2. Inverting output (positive logic output) – 1 and 4 are connected.
3. Non-inverting input (no input resistor – negative logic input) – only 5 is connected.
4. Inverting input (input resistor to V_{SS} – positive logic input) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD} – negative logic input) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and 2 non-inverting outputs the connection would be made as follows:

   Inputs – 2 and 6 are connected
   Outputs – 1, 3, 8 and 9 are connected or
   1, 3, 8 and 10 are connected

   If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

It should be noted that all internal logic and processing is performed in negative logic, i.e., "1" equals V_{DD} and "0" equals V_{SS}. For positive logic conversion, the inverted options should be selected.

TTL compatibility is obtained by $V_{DD} = -10V \pm 5\%$ and $V_{SS} = 5V \pm 5\%$. An external 12K resistor should be used on all outputs to insure the logic "0" state (V_{OL}).



4001 Available Metal Option for Each I/O Pin.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

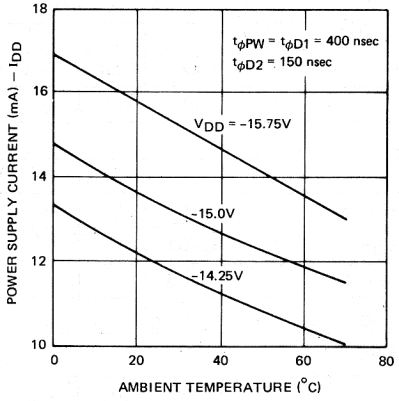
T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
SUPPLY CURRENT						
I_{DD}	Average Supply Current		15	30	mA	T_A = 25°C
INPUT CHARACTERISTICS – ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS – ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT} = V_{SS} -.5V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage, Inverting Input	V_{DD}		V_{SS}-4.2	V	
V_{IL}	Input Low Voltage, Non-inverting Input	V_{DD}		V_{SS}-6.5	V	
V_{IL}	CL Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
R_I	Input Resistance, if Used	10	18	35	kΩ	R_1 tied to V_{SS}; V_{IN} = V_{SS} -3V
R_1[1]	Input Resistance, if Used	15	25	40	kΩ	R_1 tied to V_{DD}; V_{IN} = V_{SS} -3V
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance		1.2	2	kΩ	V_{OUT} = V_{SS} -.5V
I_{OL}	I/O Output "1" Sink Current	2.5	5		mA	V_{OUT} = V_{SS} -.5V
I_{OL}[2]	I/O Output "1" Sink Current	0.8	3		mA	V_{OUT} = V_{SS} -4.85V
V_{OL}	I/O Output Low Voltage	V_{SS}-12		V_{SS}-6.5	V	I_{OUT} = 50μA
CAPACITANCE						
C_ϕ	Clock Capacitance		8	15	pF	V_{IN} = V_{SS}
C_{DB}	Data Bus Capacitance		9.5	15	pF	V_{IN} = V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN} = V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN} = V_{SS}

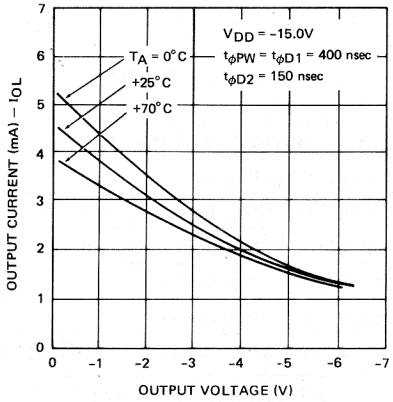
Notes: 1. R_I is large signal equivalent resistance to (V_{SS}-12) V.
2. For TTL compatibility, use 12kΩ external resistor to V_{DD}.

Typical D.C. Characteristics

POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{SS} - V_{DD} = 15V \pm 5\%$

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Times			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{IS}	I/O Input Set-Time	50			ns	
t_{IH}	I/O Input Hold-Time	100			ns	
t_D	I/O Output Delay			1500	ns	C_{OUT} = 100pF
t_C[4]	I/O Output Lines Delay on Clear			1500	ns	C_{OUT} = 100pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. CL on the 4001 is used to asynchronously clear the output flip-flops associated with the I/O lines.

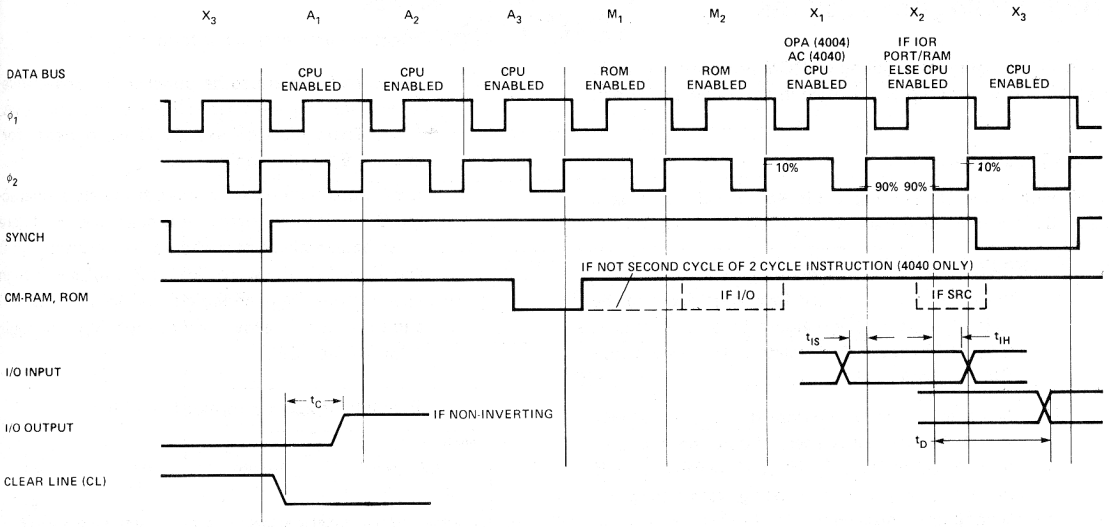


Figure 1. Timing Diagram

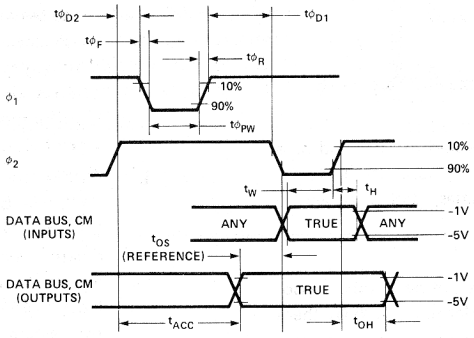


Figure 2. Timing Detail

Programming Instructions

To insure optimum handling of ROM programs and avoid delays, programs should be specified in the following format.

Paper Tape Format*

A 1" wide paper tape using 8 bit ASCII code, such as a model 33ASR teletype produces:

A. Preamble

1. Preceding the first word field and following the last word field, there should be a leader/trailer length of at least 25 characters. This should consist of rubout punches.

2. Included in the tape before the leader, and preceded by another leader, should be the customer's complete telex or twx number and if more than one pattern is being transmitted, the ROM pattern number.

3. The first ROM pattern preamble field is the device type number or ROM number. The field should be framed by an "I" and "–"

   I4001–

   This should be followed by the chip select information encoded in decimal (two digits), and enclosed by "C" and "S", as in

   "ChhS"

   The valid select digits for the 4001 are 0–15

   "C0S" – "C15S"

   Finally, the I/O options would be specified on a port-by-port basis with the connections to be made separated by commas, and enclosed in parentheses:

   "(n1, n2, n3 . . .)".

   where (n1, n2 . . .) are the option numbers associated with one I/O line. Hence, for a 4001 there will be four bracketed collections of I/O options. Each I/O pin has a series of 10 possible connections. These connections are consecutively numbered from 1-10. It is these numbers that should be in parentheses for each I/O pin.

   Example: "( )" indicates no connection
   "(1)" indicates only #1
   "(2,5,7)" indicates connections #2, 5 and 7.

   I/O options should be placed on the tape sequentially for the 4001 from I/O0–I/O3(4). Always avoid illegal combinations.

NOTE: Cards may also be submitted.

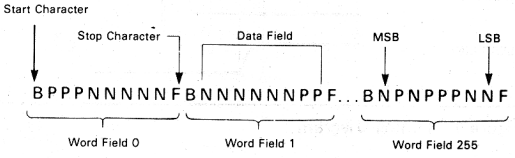
B. ROM Code

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.

2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F. Within the word field, a P results in a high level output (V_{SS} or logic 0 for MCS-40 CPUs) and a N results in a low level output (V_{DD} or logic 1 for MCS-40 CPUs).

   Example of 256 x 8 format (N=256):



3. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. It may be helpful to insert the word number (as a comment) at least every four word fields.

4. Within the ROM pattern words a character, "X", may be used. Where "P" and "N" indicate a "0" and "1" setting respectively, an "X" will indicate a single bit – "Don't Care" setting. This allows the optimum default bit values to be selected by Intel. The bit value will be fixed to allow for testing. The values will be specified to the user on the Verification Listing tape.

   In the place of a standard BPNF word, a "B*nF" word may be used. This indicates that the data in the last BPNF word encountered is to be repeated for the next n words ($1 \leq n \leq 1023$). Note that if a repeat count of 4 is given in word position 10, then words 10, 11, 12, and 13 will be repeats of word 9 (except for Don't Care bits which might conceivably have different assigned values).

   To indicate that an entire block (such as the remainder of a ROM) is not used (i.e., Don't Care), a word of Don't Care data can be followed by the remaining word count in a repeat count form.

MCS® CUSTOM ROM ORDER FORM

4001 ROM

CUSTOMER_____

P.O. NUMBER_____

DATE_____

For Intel use only

S#_____ PPPP_____

STD_____ ZZ_____

_____ DD_____

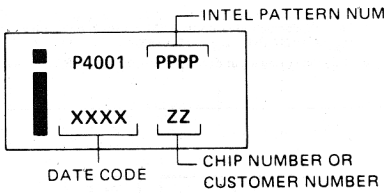
APP_____ DATE_____

All custom 4001 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4001), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).

CUSTOMER NUMBER _____



MASK OPTION SPECIFICATIONS

A. CHIP NUMBER _____.
(Must be specified—any number from 0 through 15—DD).

B. I/O OPTION – Specify the connection numbers for each I/O pin (next page). Examples of some of the possible I/O options are shown below:

EXAMPLES – DESIRED OPTION/CONNECTIONS REQUIRED

1. Non-inverting output – 1 and 3 are connected.
2. Inverting output – 1 and 4 are connected.
3. Non-inverting input (no input resistor) – only 5 is connected.
4. Inverting input (input resistor to V_{SS}) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD}) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and two non-inverting outputs, the connection would be made as follows:

   Inputs – 2 and 6 are connected
   Outputs – 1, 3, 8, and 9 are connected or
   1, 3, 8, and 10 are connected

   If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

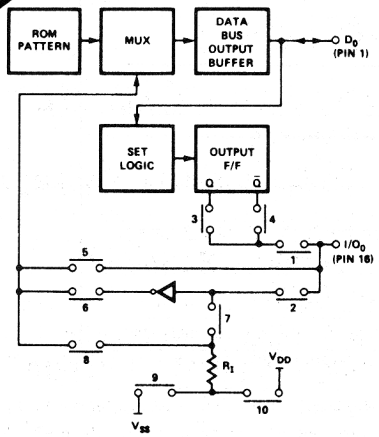
C. 4001 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Based on the particular customer pattern, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

Note that:

NOP = BPPPP PPPPF = 0000 0000

4001 I/O Options

SAMPLE

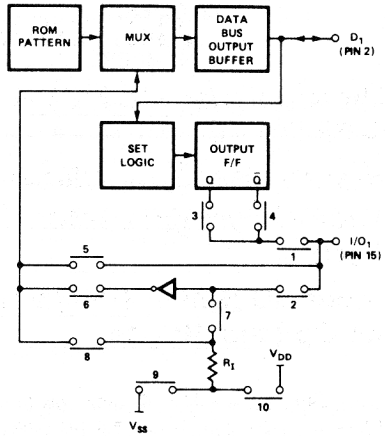


I/O_0 (PIN 16)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

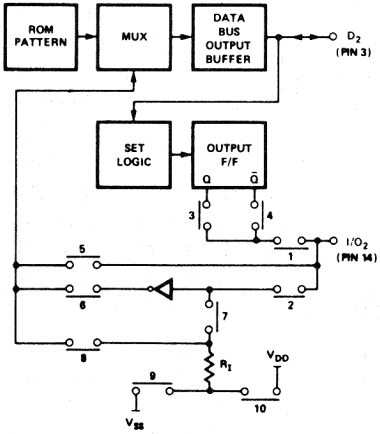


I/O_1 (PIN 15)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

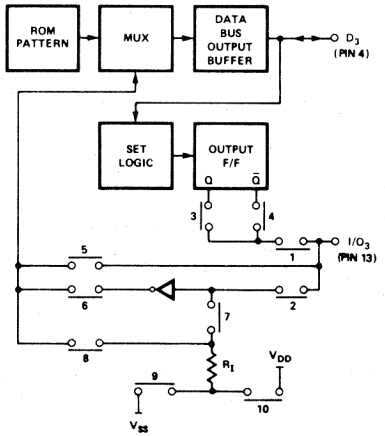


I/O_2 (PIN 14)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).



I/O_3 (PIN 13)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

4002

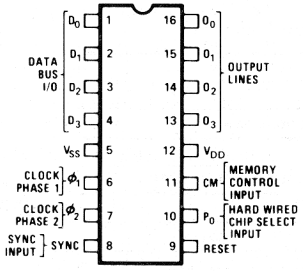
320 BIT RAM AND 4 BIT OUTPUT PORT

- **Four Registers of 20 4 Bit Characters**
- **Direct Interface to MCS-40™ 4 Bit Bus**
- **Output Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available With -40° to +85°C Operating Range**

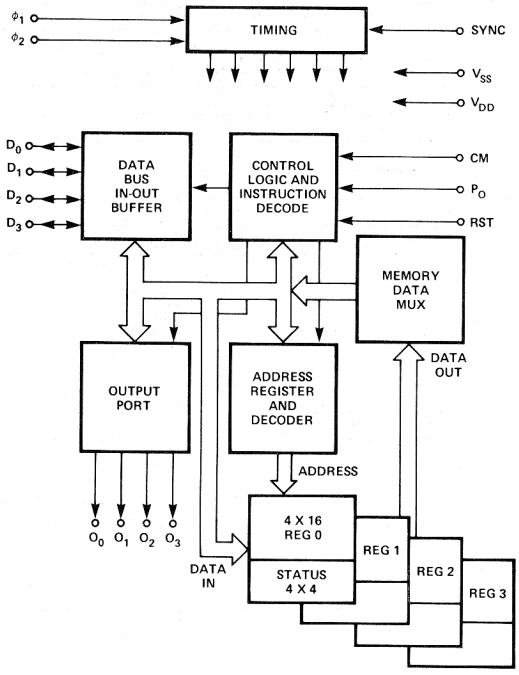
The 4002 performs two distinct functions. As a RAM it stores 320 bits arranged in 4 registers of twenty 4 bit characters each (16 main memory characters and 4 status characters). As a vehicle of communication with peripheral devices, it is provided with 4 output lines and associated control logic to perform output operations. The 4002 is a PMOS device and is compatible with all MCS-40™ components.

The 4002 is available in two options, the 4002-1 and 4002-2. Along with an external pin connected to either V_{DD} or V_{SS}, a two bit chip selection address is provided allowing a maximum of 1280 bits of 4002 RAM on a single MCS-40 CM-RAM line. Thus, the four CM-RAM lines give a maximum of 5120 bits of 4002 RAM in an MCS-40 system.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation	Description of Function
1-4	D_0-D_3	Bidirectional data bus. All address, instruction and data communication between processor and the RAM MEMORY or the output port is transmitted on these 4 pins.
5	V_{SS}	Most positive supply voltage.
6-7	ϕ_1-ϕ_2	Non-overlapping clock signals which are used to generate the basic chip timing.
8	SYNC	Synchronization input signal driven by SYNC output of processor.
9	RESET	RESET input. A logic negative level (V_{DD}) applied to the chip will cause a clear of all output and control static flip-flops and will clear the RAM array. To completely clear the memory, RESET must be applied for at least 32 instruction cycles (256 clock periods) to allow the internal refresh counter to scan the memory. During RESET the data bus output buffers are inhibited (floating condition).
10	Po	The chip number for a 4002 is assigned as follows:

Chip No.	4002 Option	P_0	SRC ADDRESS (RRR EVEN) D_3 D_2
0	4002-1	V_{SS}	0 0
1	4002-1	V_{DD}	0 1
2	4002-2	V_{SS}	1 0
3	4002-2	V_{DD}	1 1

11	CM	Command input driven by CM-RAM output of processor. Used for enabling the device during the decoding SRC and instructions.
12	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V ± 5%.
13-16	O_3-O_0	Four bit output port used for transferring data from the CPU to the users system. The outputs are buffered and data remains stable after the port has been loaded. This port can be made low power TTL compatible by placing a 12K pull-down resistor to V_{DD} on each pin.

Functional Description

The twenty 4 bit characters for each 4002 register are arranged as follows:

1. 16 characters addressable by an SRC instruction. Four 16 character registers constitute the "main" memory.
2. 4 characters addressable by specific RAM instructions. Four 4 character registers constitute the "status character" memory.

The status character location (0 through 3) as well as the operation to be performed on it are selected by the OPA portion of the I/O and RAM instructions.

The RAM Registers Locations, Status Characters, and Output Port are select and accessed with a corresponding RAM Instruction.

There can be up to four RAMS per RAM Bank (CM-RAM). There can be four RAM banks per system without decoding or 8 with decoding.

Bank switching is accomplished by the CPU after receiving a "DCL" (designated command line) instruction. Prior to execution of the DCL instruction the desired CM-RAM code has been stored in the accumulator (for example through an LDM instruction). During DCL the CM-RAM code is transferred from the accumulator to the CM-RAM register. The RAM bank is then selected starting with the next instruction.

If no DCL is executed prior to SRC, the CM-RAM_0 will automatically be activated at the X_2 state of the instruction cycle provided that RESET was applied at least once to the system (most likely at the start-up time).

MCS 4/40

Instruction Execution

An SRC (Send Register Control) instruction is executed to select a RAM and a character within that RAM (for a RAM read or write instruction) prior to the succeeding RAM or I/O instruction's execution.

The eight bits of the register pair addressed by the SRC instruction are interpreted as follows:

a. The first four bits sent out at X_2 time select one out of four chips and one out of four registers. The two higher order bits (D_3, D_2) select the chip and the two lower order bits (D_1, D_0) select the register.

b. The second 4-bits (X_3 time) select one 4-bit character out of 16. The address is stored in the address register of the selected chip (second 4 bits are not used for status character reads or writes or for I/O output instructions).

The following RAM and I/O output instructions are executed by the 4002.

1. RDM Read RAM character

   The content of the previously selected RAM main memory character is transferred to the accumulator. The 4 bit data in memory is unaffected.

2. RDO-3 Read RAM status characters 0-3

   The 4 bits of status characters 0-3 for the previously selected RAM register are transferred to the accumulator.

3. WRM Write accumulator into RAM character

   The accumulator content is written into the previously selected RAM main memory character location.

4. WRO-3 Write accumulator into RAM status characters 0-3

   The content of the accumulator is written into the RAM status characters 0-3 of the previously selected RAM register.

5. WMP Write memory port

   The content of the accumulator is transferred to the RAM output port of the previously selected RAM chip. The data is available on the output pins until a new WMP is executed on the same RAM chip. The content of the ACC and the carry/link are unaffected. (The LSB bit of the accumulator appears on O_0, Pin 16 of the 4002.)

6. ADM Add from memory with carry

   The content of the previously selected RAM main memory character is added to the accumulator with carry. The RAM character is unaffected.

7. SBM Subtract from memory with borrow

   The content of the previously selected RAM character is subtracted from the accumulator with borrow. The RAM character is unaffected.

Timing Considerations

Presence of CM-RAM during X_2 tells 4002's that an SRC instruction was received. For a given combination of data at X_2 on D_2, D_3, only the chip with the proper option and P_0 state will be ready for the I/O or RAM operation that follows.

When an I/O or RAM instruction is received by the CPU, the CPU will activate one CM-RAM line during M_2, in time for the 4002's to receive the OPA (2nd part of the instruction), which will specify the I/O or RAM operation to be performed.

In the I/O mode of operation, the selected 4002 chip (by SRC), after receiving the OPA of an I/O instruction (CM-RAM activated at M_2), will decode the instruction.

If the instruction is WMP, the data present on the data bus during $X_2 \cdot \phi_2$ will set the output flip-flops associated with the I/O pins. That information will be available until next WMP for peripheral devices control.

In the RAM mode, the operation is as follows: When the CPU receives an SRC instruction, it will send out the content of the designated index register pair during X_2 and X_3 and will activate one CM-RAM line at X_2 for the previously selected RAM bank.

All RAM mode instructions will be executed during the X_2 and X_3. The instruction decoding is performed during the M_2 time when the OPA portion of the instruction is decoded. The CM-RAM of the selected Bank is enabled at that time.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

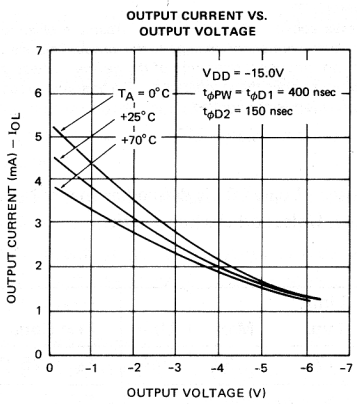
T_A = 0°C to 70°C; V_{SS}-V_{DD} = 15V ±5%; $t_{\phi PW} = t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec. Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless otherwise specified.

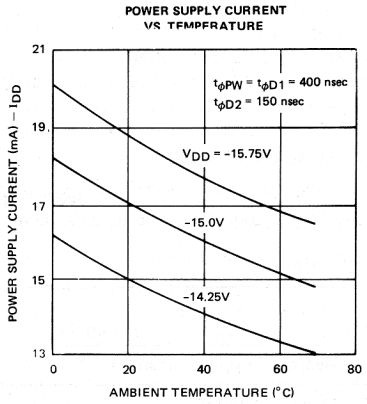
SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		17	33	mA	T_A = 25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL}=V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS – ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT}=-12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT}=V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL}=0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT}=0
R_{OH}	I/O Output "0" Resistance		1.2	2	kΩ	V_{OUT}=V_{SS}-.5V
I_{OL}	I/O Output "1" Sink Current	2.5	5		mA	V_{OUT}=V_{SS}-.5V
I_{OL}[1]	I/O Output "1" Sink Current	0.8	3		mA	V_{OUT}=V_{SS}-4.85V
V_{OL}	I/O Output Low Voltage	V_{SS}-12		V_{SS}-6.5	V	I_{OUT}=50μA
CAPACITANCE						
C_{ϕ}	Clock Capacitance		8	15	pF	V_{IN}=V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN}=V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN}=V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN}=V_{SS}

Note: 1. For TTL compatibility, use 12kΩ external resistor to V_{DD}.

Typical D.C. Characteristics





A.C. Characteristics

T_A = 0°C to 70°C, V_{SS}-V_{DD} = 15V ±5%.

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t_{\phi R}$	Clock Rise Time			50	ns	
$t_{\phi F}$	Clock Fall Times			50	ns	
$t_{\phi PW}$	Clock Width	380		480	ns	
$t_{\phi D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t_{\phi D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT}=20pF
t_D	I/O Output Delay			1500	ns	C_{OUT}=100pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

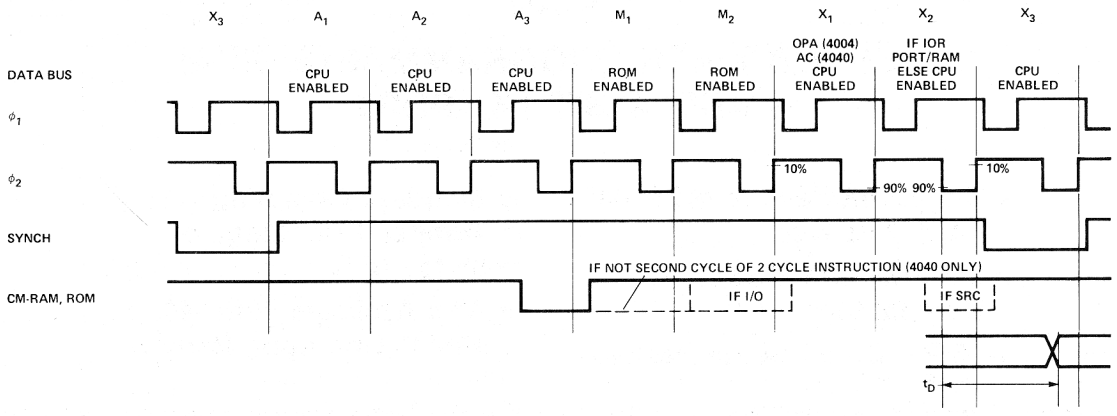


Figure 1. Timing Diagram.

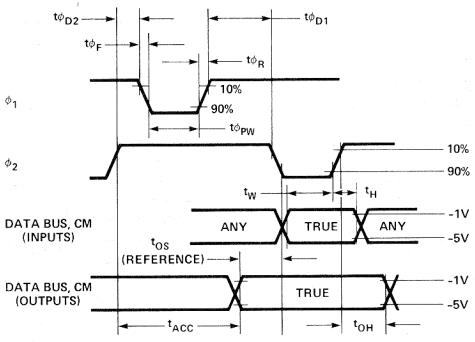


Figure 2. Timing Detail.

4003

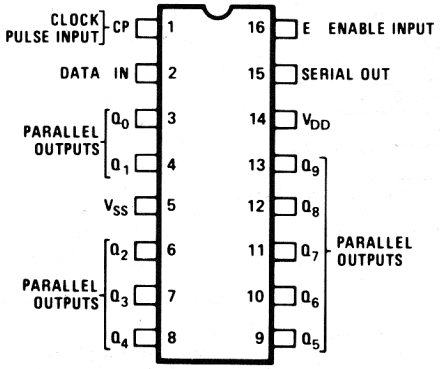
10 BIT SHIFT REGISTER/OUTPUT EXPANDER

- **10 Bit Serial-In/Parallel Out**
- **Serial-Out Capability for Additional I/O Expansion**
- **16 Pin Dual-In-Line Package**
- **Easy Expansion of I/O Output Capability**
- **Enable Output Control**
- **Standard Operating Temperature Range of 0° to 70°C**

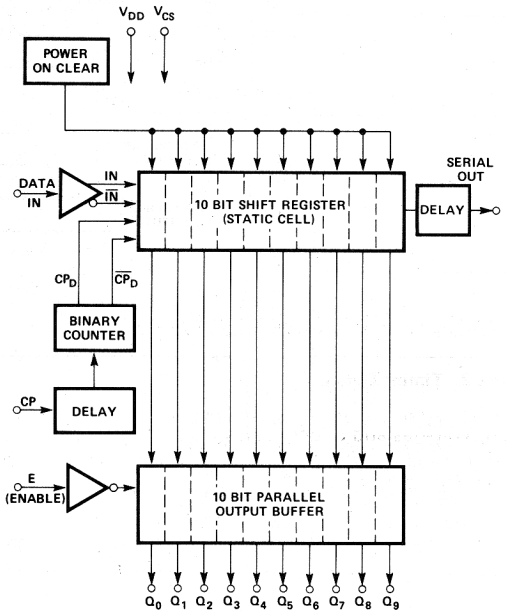
The 4003 is a 10 bit serial-in, parallel-out, serial-out shift register with enable logic. The 4003 is used to expand the number of ROM and RAM I/O ports to communicate with peripheral devices such as keyboards, printers, displays, readers, teletypewriters, etc.

The 4003 is a single phase static shift register; however, the clock pulse (CP) maximum width is limited to 10 msec. Data-in and CP can be simultaneous. To avoid race conditions, CP is internally delayed.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation	Description of Function
1	CP	The clock pulse input. A "0" (V_{SS}) to "1" (V_{DD}) transition will shift data in.
2	DATA IN	Serial data input line.
3	O_0	Parallel data output lines, when enabled. Each pin may be made TTL compatible with a 5.6K pull-down resistor to V_{DD}.
4	O_1	
6	O_2	
7	O_3	
8	O_4	
9	O_5	
10	O_6	
11	O_7	
12	O_8	
13	O_9	
5	V_{SS}	Most positive supply voltage.
14	V_{DD}	Main supply voltage value must be V_{SS} - 15.0V ± 5% (-10v for TTL operation)
15	Serial out	Serial data output.
16	E	Enable, when E = "1" (V_{DD}) the output lines contain valid data. When E = "0" (V_{SS}) the output lines are at V_{SS}.

Functional Description

The 4003 is designed to be typically appended to an MCS-40 I/O port. This can be the I/O port of a 4001, 4002, 4289, 4308, or a 4265. One I/O line is assigned to be the Enable (E), another the Clock (CP), and still another the Serial Data-Input. For example, to access the 4003 a subroutine of sequential outputs consisting of Data, clock pulse on, Enable – followed by an output of clock pulse off and Enable, will serially load the 4003.

Data is loaded serially and is available in parallel on 10 output lines which are accessed through enable logic. When enabled (E = 1 -- V_{DD}), the shift register contents are read out; when not enabled (E = 0 -- V_{SS}), the parallel-out lines are at Logic "0" (V_{SS}). The serial-out line is not affected by the enable logic to allow longer word cascading.

Data is also available serially permitting an indefinite number of similar devices to be cascaded together to provide shift register length multiples of 10.

The data shifting is controlled by the CP signal. An internal power-on-clear circuit will clear the shift register (outputs = 0 or V_{SS}) between the application of the supply voltage and the first CP signal.

The 4003 output buffers are useful for multiple key depression rejection when a 4003 is used in conjunction with a keyboard. In this mode if up to three output lines are connected together, the state of the output is high (Logic "0" or V_{SS}) if at least one line is high.

Another typical application of the 4003 is for Keyboard or Display Scanning where a single bit of Logic "1" is shifted through the 4003 and is used to activate the various digits, keyboard rows, etc.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

T_A = 0°C to +70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec, $t_{\phi D2}$ = 150 nsec, unless otherwise specified.

Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}), Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}).

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		5.0	8.5	mA	t_{WL} = t_{WH} = 8μsec; T_A = 25°C
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3		
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
I/O OUTPUT CHARACTERISTICS						
I_{OL}	Parallel Out Pins Sinking Current, "1" Level	0.6	1.0		mA	V_{OUT} = 0V. For TTL compatibility a 5.6KΩ (±10%) resistor between output and V_{DD} should be added.[2]
I_{OL}	Serial Out Sinking Current, "1" Level	1.0	2.0		mA	V_{OUT} = 0V
V_{OL}	Output Low Voltage	V_{SS}-11	V_{SS}-7.5	V_{SS}-6.5	V	I_{OL} = 10μA
R_{OH}	Parallel-Out Pins Output Resistance "0" Level		400	750	Ω	V_{OUT} = -0.5V
R_{OH}	Serial Out Output Resistance "0" Level		650	1200	Ω	V_{OUT} = -0.5V

Notes: 1. Typical values are to T_A = 25°C and Nominal Supply Voltages.

2. For TTL compatibility on the I/O lines the supply voltages should be V_{DD} = -10V ±5%; V_{SS} = +5V ±5%.

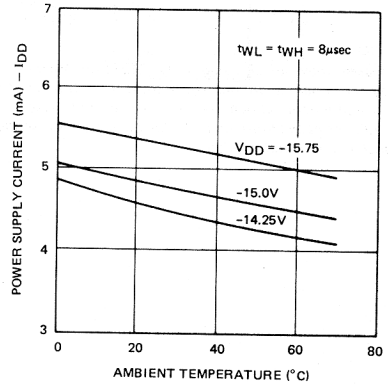
CAPACITANCE

f = 1 MHz; V_{IN} = 0V; T_A = 25°C; Unmeasured Pins Grounded.

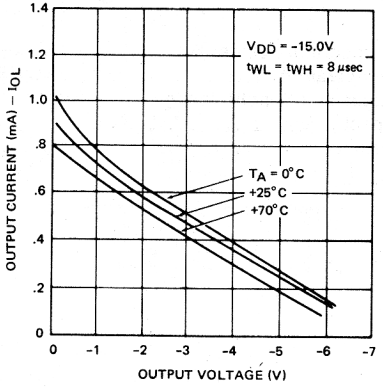
Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF

Typical D.C. Characteristics

POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



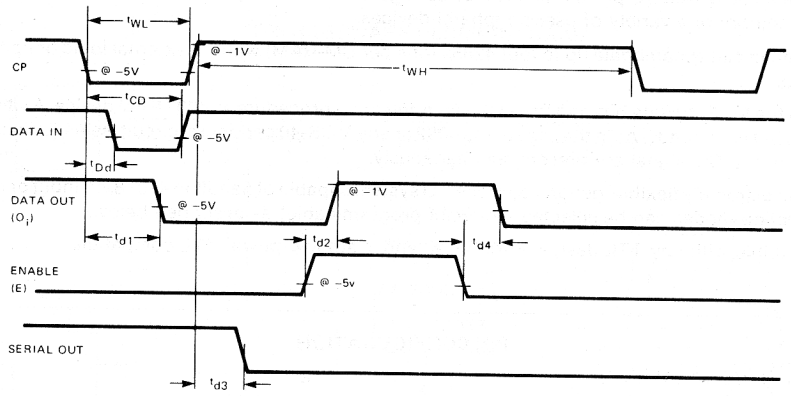
A.C. Characteristics

T_A = 0°C to +70°C; V_{DD} = -15 ±5%, V_{SS} = GND

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{WL}	CP Low Width	6		10,000	μsec	
t_{WH}[1]	CP High Width	6			μsec	
t_{CD}	Clock-On to Data-Off Time	3			μsec	
t_{Dd}[2]	CP to Data Set Delay			250	nsec	
t_{d1}	CP to Data Out Delay	250		1750	nsec	
t_{d2}	Enable to Data Out Delay			350	nsec	C_{OUT} = 20pF
t_{d3}	CP to Serial Out Delay	200		1250	nsec	C_{OUT} = 20pF
t_{d4}	Enable to Data Out Delay			1.0	μsec	C_{OUT} = 20pF

Notes: 1. t_{WH} can be any time greater than 6μsec.
2. Data can occur prior to CP.

Timing Diagram

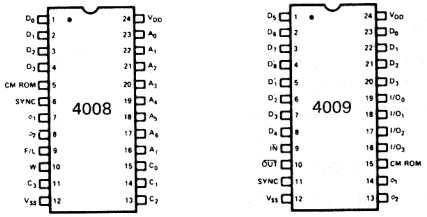


4008/4009
STANDARD MEMORY AND I/O INTERFACE SET

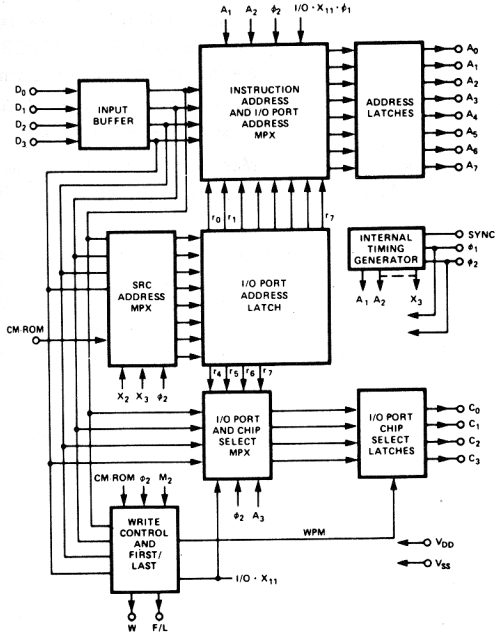
- **Direct Interface to Standard Memories**
- **Allows Write Program Memory**
- **24 Pin Dual In-Line Packages**
- **Standard Operating Temperature Range of 0° to 70 °C**

The standard memory and I/O interface set (4008/4009) provides the complete control functions performed by the 4001 or 4308 in MCS-40™ systems. The 4008/4009 are completely compatible with other members of the MCS-40 family. All activity is still under control of the CPU. One set of 4008/4009 and several TTL decoders is sufficient to interface to 4K words of program memory, sixteen four-bit input ports and sixteen four-bit output ports.

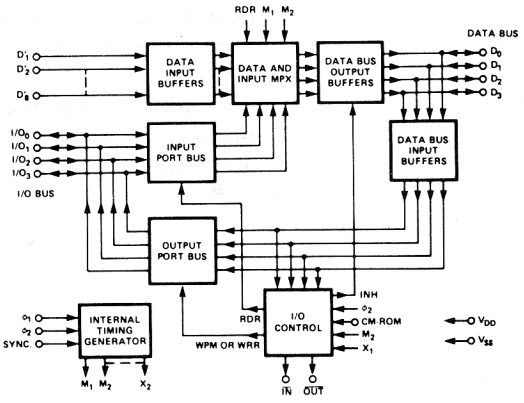
PIN CONFIGURATIONS



4008 BLOCK DIAGRAM



4009 BLOCK DIAGRAM



Pin Description

4008

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
7-8	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
6	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
5	CM-ROM/Neg.	Command input driven by CM-ROM output of processor. Used for decoding SRC and I/O instructions.
23-16	A_0-A_7/Pos.	Address output buffers. The demultiplexed address values generated by the 4289 from the address data supplied by the processor at A_1 and A_2.
15-13, 11	C_0-C_3/Pos.	Chip select output buffers. The address data generated by the processor at A_3, or during an SRC are transferred here.
9	F/L/Neg.	Output signal generated by the 4008 to indicate which half-byte of PROGRAM MEMORY is to be operated on.
10	W/Pos.	Output signal, active low, generated by the 4008 when the processor executes a WPM instruction.
12	V_{SS}	Most positive supply voltage.
24	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.

4009

Pin No.	Designation/ Type of Logic	Description of Function
23-20	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
5-8, 1-4	D'_1-D'_8/Pos.	The eight bits of instruction from the program memory are transferred on these 4009 pins (most significant bit is D'_8).
14-13	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
11	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
15	CM-ROM/Neg.	Command input driven by CM-ROM output of Processor.
9	IN/Neg.	Output signal, active low, generated by the 4289 when the processor executes an RDR instruction.
10	OUT/Neg.	Output signal, active low (V_{DD}), generated by the 4009 when the processor executes a WRR instruction.
19-16	I/O_0-I/O_3/Pos.	Bidirectional I/O data bus. Data to and from I/O ports or data to write PROGRAM MEMORY are transferred via these pins.
23	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.
12	V_{SS}	Most positive supply voltage.

Functional Description

The 4008 is the address latch chip which interfaces the 4004 or 4040 to standard PROMs, ROMs and RAMs used for program memory. The 4008 latches the low order eight bits of the program address sent out by the CPU during A1 and A2 time. During A3 time it latches the high order four bits of the program address from the CPU. The low-order eight bits of the program address are then presented at pins A0 through A7 and the high-order four bit (also referred to as page number) are presented at pins C0 through C3. These four bits must be decoded externally and one page of program memory is selected.

The 4009 then transfers the eight bit instruction from program memory to the CPU four bits at a time at M1 and M2. The command signal sent by the CPU activates the 4009 and initiates this transfer.

When the CPU executes an SRC (Send Register Control) instruction, the 4008 responds by storing the I/O address in its eight bit SRC register. The content of this SRC register is always transferred to the address lines (A0 through A7) and the chip select lines (C0 through C3) at X1 time. The appropriate I/O port is then selected by decoding the chip select lines. The IN and OUT lines of the 4009 indicate whether an input or output operation will occur.

The 4009 is primarily an instruction and I/O transfer device. When the CPU executes an RDR (Read ROM Port) instruction, the 4009 will send an input strobe (pin 9) to enable the selected input port. It also enables I/O input buffers to transfer the input data from the I/O bus to the data bus. When the 4009 interprets a WRR (Write ROM Port) instruction, it transfers output data from the CPU to the I/O bus and sends an output strobe (pin 10) to enable the selected output port.

The WPM (Write Program Memory) instruction is used in conjunction with the 4008/4009 to write data into the RAM program memory. When an instruction is to be stored in RAM program memory, it is written in two four-bit segments. The F/L signal from the 4008 keeps track of which half is being written. When the CPU executes a WPM instruction, the chip select lines of the 4008 are jammed with "1111". In the system design this should be designated as the RAM channel. The W line on the 4008 is also activated by the WPM instruction. The previously selected SRC address on line A0 through A7 of the 4008 becomes the address of the RAM word being written. By appropriately decoding the chip select lines, the W line, and F/L, the write strobes can be generated for the memory.

The F/L line is initially high (V_{SS}) when power comes on. It then pulses low (V_{DD}) when every second WPM is executed. A high (V_{SS}) on the F/L lines means that the first four bits (OPR) are being written, and a low means that the last four bits (OPA) are being written. The 4009 transfers the segment of the instruction to the I/O bus at X2 of the WPM instruction. The SRC address sent to RAM is only 8 bits. When more than one page of RAM (256 bytes) is being written, an output port must be used to supply additional address lines for higher order addresses.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to V_{SS}	+0.5V to -20V
Power Dissipation	1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current (4008 only)		10	20	mA	T_A = 25°C
I_{DD}	Average Supply Current (4009 only)		13	30	mA	T_A = 25°C
INPUT CHARACTERISTICS–ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS–ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitance Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
I_{OL}[1]	Address Line Sinking Current (4008 only)	7	13		mA	V_{OUT} = V_{SS}
I_{OL}	In, Out, F/L, Chip Select	1.6	4		mA	V_{OUT} = V_{SS} -4.85
I_{OL}[2]	W Output, Sinking Current (4008 only)	2.5	5		mA	V_{OUT} = V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level (4008 only)		150	250	Ω	V_{OUT} = V_{SS} -.5V
R_{OH}	Address, Chip Select Output Resistance, "0" Level (4008 only)		.6	1.2	kΩ	V_{OUT} = V_{SS} -.5V
R_{OH}	Output Resistance, Data Line "0" Level (4009 only)		130	250	Ω	V_{OUT} = V_{SS} -2V
I_{CF}[3]	Address, C/S Output "1" Clamp Current (4008 only)			16	mA	V_{OUT} = V_{SS} -6V
I_{CF}[3]	In, Out "1" Clamp Current (4009 only)			16	mA	V_{OUT} = V_{SS} -6V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}[4]	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (4009 only)	V_{DD}		V_{SS}-4.2	V	
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance (4009 only)		.25	1.0	kΩ	V_{OUT} = V_{SS} -.5
I_{OL}	I/O Output "1" Sink Current (4009 only)	5	12		mA	V_{OUT} = V_{SS} -.5V
I_{OL}	I/O Output "1" Sink Current (4009 only)	1.6	4		mA	V_{OUT} = V_{SS} -4.85V
I_{CF}	I/O Output "1" Clamp Current (4009 only)			16	mA	V_{OUT} = V_{SS} -6V
CAPACITANCE						
C_{ϕ}	Clock Capacitance		8	15	pF	V_{IN} = V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN} = V_{SS}
C_{IN}	Input Capacitance (4008 only)			10	pF	V_{IN} = V_{SS}
C_{IN}	Input Capacitance (4009 only)			15	pF	V_{IN} = V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN} = V_{SS}

Notes: 1. The address lines will drive a TTL load if a 470Ω resistor is connected in series between the address output and the TTL input.
2. A 6.8kΩ resistor must be connected between Pin W and V_{DD} for TTL capability.
3. Resistors in series with TTL inputs may be required to limit current into V_{DD} or V_{SS} from TTL input clamp diodes.
4. TTL V_{OH} = 2.4V will ensure 4009 V_{IH} = V_{SS} -1.5 via the 4009 latch. Refer to Figure 3.

A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{SS} - V_{DD} = 15V \pm 5\%$

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Times			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay $\phi 1$ to ϕ_2	400		500	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500 pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{A1}	Address to Output Delay at A_1, X_1 (4008)			580	ns	C_L = 250pF
t_{A2}	Address to Output Delay A_2 (4008)			580	ns	C_L = 250pF
t_{CS}	Chip Select Output Delay at A_3 (4008)			300	ns	C_L = 50pF
t_{WD}	W Output Delay (4008)			600	ns	C_L = 100pF
t_{FD}	F/L Output Delay (4008)	0.1		1	μs	C_L = 100pF
t_{WI}	Data In Write Time (4009)	470			ns	C_L = 200pF on data bus
t_D	I/O Output Delay (4009)			1.0	μs	C_L = 300pF
t_{S1}	IN Strobe Delay (4009)			450	ns	C_L = 50pF
t_{S2}	OUT Strobe Delay (4009)			1.0	μs	C_L = 50pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

Timing Diagram

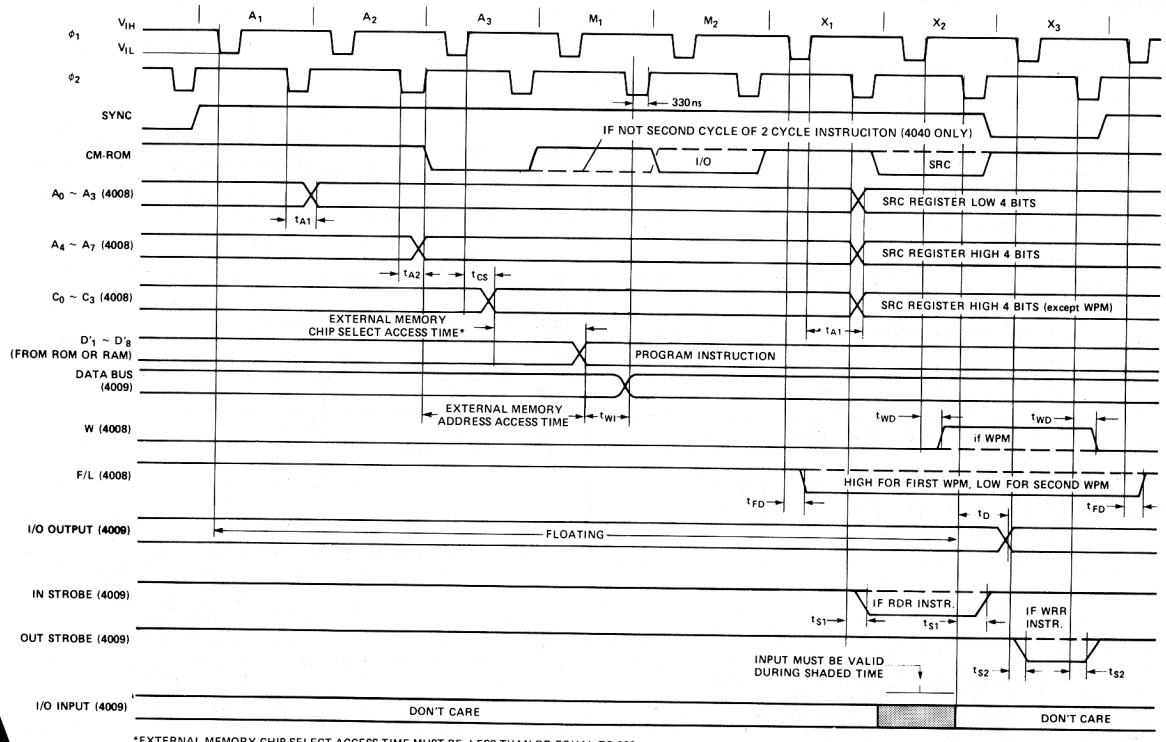


Figure 1. 4008 and 4009 Timing Diagram.

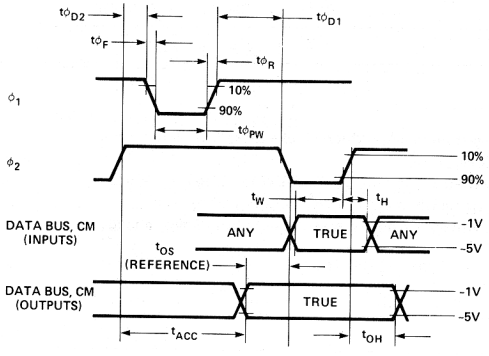
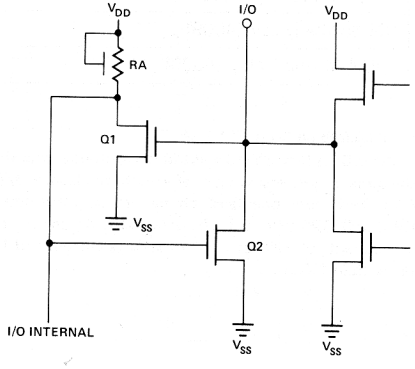


Figure 2. MCS-40 Timing Detail.



EXPLANATION:

WITH V_{SS} = +5V and V_{DD} = -10V, AN EXTERNAL TTL INPUTTING TO THE 4009 ON THE I/O LINE, RAISES THE I/O LINE TO 2.4V. THE Q1-RA INVERTER TURNS "OFF" AND Q2 PULLS THE I/O LINE TO V_{SS}. A LOW TTL SIGNAL OVERRIDES Q2. IF THE TTL OUTPUT GOES TO THE THIRD STATE, THE EXTERNAL I/O LINES REMAIN HIGH THROUGH Q2.

THE PURPOSE OF THIS CIRCUIT IS TO REMOVE RESISTORS TO $V_{CC} = V_{SS}$ ON TTL OUTPUTS, AS R_I DOES ON 4001/4308 INPUT PORTS.

Figure 3. 4009 I/O Latch.